

SIMULATED TEMPERATURE DEPENDENCY OF SEU SENSITIVITY IN A 0.5 μm
CMOS SRAM

By

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I would like to dedicate this research to my family without whose support none of my accomplishments would have been possible.

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LIST OF ACRONYMS

Acronym	Meaning
BJT	Bipolar Junction Transistor
CMOS.....	Complimentary Metal Oxide Semiconductor
DD.....	Displacement Damage
DTF.....	Data Transfer Facility
GTO	Geo Transfer Orbit
GCR	Galactic Cosmic Rays
GUI.....	Graphical User Interface
HBT.....	Heterojunction Bipolar Transistor
LEO.....	Low Earth Orbit
LET	Linear Energy Transfer
nFET	n-channel Field Effect Transistor
PDK.....	Process Design Kit
pFET	p-channel Field Effect Transistor
SEE.....	Single Event Effect
SEU.....	Single Event Upset
SiGe.....	Silicon Germanium
SRAM.....	Static Random Access Memory
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose

CHAPTER I

INTRODUCTION

The focus of this research is to study the temperature dependency of Single Event Upset (SEU) sensitivity for a Static Random Access Memory (SRAM) cell created in the commercial IBM 5AM 0.5 μm BiCMOS process technology. For electronics intended to operate in space systems, several aspects of the devices must be considered. They are the size, weight, cost, power consumption, and ability to operate in extreme environments. For commercial satellite launches, it currently costs around \$4,000 USD per pound to launch into Low Earth Orbits (LEO) and around \$10,000 USD per pound to launch into Geo Transfer Orbit (GTO)¹. By eliminating bulky and wasteful equipment with advanced technology, the power and weight of a given system can be reduced which in turn reduces the cost and enhance performance. One such technology is SiGe BiCMOS. This technology allows for efficient integration of analog, digital, and mixed signal functions without moving to the leading edge generation. Therefore, it is important to understand the environments, device models, and simulation tools that impact the successfulness of the mission. The consequences could lead to a loss of time, energy, and resources.

The requirements of space exploration include an ability to withstand extreme conditions, as well as the exposure to radiation effects. They are subjected to varying degrees of damage due to the natural space environment. Particles in space create ionizing radiation which contributes to Total Ionizing Dose (TID), Single Event Effects (SEEs), and Displacement Damage (DD). While protons are responsible for all areas of

radiation damage, electrons contribute to total-dose and displacement damage; heavy ions cause SEEs. Additionally, electronics may be required to operate over large temperature ranges. In fact, implementing electronics that can function across these temperature ranges can reduce the need for environmental control hardware such as hot boxes. SiGe BiCMOS has attributes of wide temperature operation capabilities. The Heterojunction Bipolar Transistors (HBTs) have shown to have inherent resistance to TID radiation exposure².

Of these ranges of temperature environments to be considered, one facet, a subset of focus for this thesis, is the sensitivity to SEE and how temperature affects the response. In particular, it is the purpose of this research to investigate the temperature sensitivity of SEUs in a digital SRAM cell designed and implemented from the CMOS library of the BiCMOS process technology, particularly at reduced operating temperatures.

In the context of the target system, error management is planned for key memory blocks. However, excessive sensitivity at the cell level may render these techniques overly challenged and perhaps ineffective. It is important to evaluate the expected level of sensitivity at the memory cell in order to determine the need for any possible hardening by design. Only limited data is available, and none for this technology or design. The use of simulations will give estimations of sensitivity, including the evaluation of temperature dependence, which can be used to determine the need for design modifications. Currently, limited data and preliminary modeling suggests that reduced temperature will exacerbate SEU sensitivity. The approach of this work will be to apply newly implemented temperature dependent models with an interface between the

NanoTCAD 3D device simulators and the Cadence Spectre circuit simulator. These tools will be used to evaluate the temperature dependency of SEU sensitivity of an SRAM cell.

The use of Technology Computer Aided Design (TCAD) has been an effective tool in understanding the nature of a device, at the physical level, as it is bombarded by a particle causing a Single Event. These simulations and device models require high accuracy in order to make predictions on how the device will function. Without accurate predictions of these models, one will risk catastrophic failure of these electronics. Thus, understanding the simulation environment, the modeled devices, and the simulation results are essential for the application of modern electronics in the space environment.

Fundamentally with this technology, there is a need to understand its reaction to variable temperature environments. TCAD simulations can help in this understanding as better models are created. The newly developed mixed-mode capability, which couples TCAD directly to Spectre in order to use various compact models, will be used to study the temperature dependency of devices operating in space. It will be shown, by means of mixed-mode simulation, that the process technology under study for the digital SRAM cell will have an increase in SEU sensitivity due to the corresponding decrease in temperature.

Chapter II discusses SEE and how they affect semiconductor devices, SEU Sensitivities of SRAMs, the process technology studied in this work, and the space environment involving cold temperature dependency.

Chapter III discusses the various TCAD tools provided by CFD Research Corporation and ESI group used to create the devices under investigation and the methodology used to implement the tools.

Chapter IV shows the calibration of the TCAD n-channel Metal Oxide Semiconductor Field Effect Transistor (nFET) and p-channel Metal Oxide Semiconductor Field Effect Transistor (pFET) to the electrical characteristics of the Product Design Kits (PDKs) of the IBM SiGe 5AM 0.5 μm nFET and pFET as well as a comparison between experimental charge collection data of the 5AM nFET and pFET and simulation results of the TCAD nFET and pFET.

Chapter V describes the simulations involving the SRAM cell, using the TCAD devices and compact models, created by University of Arkansas. Mixed-mode simulation results for the SEU sensitivity of the SRAM cell, including the temperature dependency, are presented. Key findings show that a reduction in temperature from 300K to 100K results in a 30% decrease in the critical charge for the nFET and 35% for the pFET for the same reduction in temperature. Additionally, it is shown that the worst case(minimum) upset threshold for the SRAM is sufficiently above the upset threshold allowed by the mitigation strategy. Therefore, radiation hardening is not required at the cell level.

CHAPTER II

BACKGROUND

Single Event Effects

SEEs are localized effects that interact as a transient within a specific region of the device. They are caused by ionized particles interacting with a semiconductor device as the particle transfers energy to the lattice structure of the device. When an ionized particle passes through a semiconductor device, electron-hole pairs are generated as the particle slowly transverses through the active region and substrate³. The rate of this energy loss to the generation of electron-hole pairs is expressed as Linear Energy Transfer's (LET's) which have the units of MeV-cm²/mg. An important note, the particle strike may have little or no measurable effect, a circuit disruption due to the transient, a logic flip, or even irreparable damage to the device.

For the purpose of this research, the particles of most interest are the protons and heavy ions. Heavy ions are associated with solar flares from deep space, also known as Galactic Cosmic Rays (GCRs), as well as other particles with high energies. Protons can also be generated by solar flares which get trapped within the geomagnetic field⁴. Understanding how these particles interact in a single SRAM cell designed using the SiGe BiCMOS process technology will help in determining whether higher levels of hardening are required for the design of the memory block.

SEU Sensitivity of SRAMs

SEUs are a more specific topic in the general field of SEEs. An example of an SEU is shown as Fig. 1. This figure shows the voltage vs. time response as well as the current at the node where the SRAM cell was struck by an ion with (Top) a charge slightly higher than the critical charge and (Bottom) a charge slightly lower than the critical charge of the SRAM.

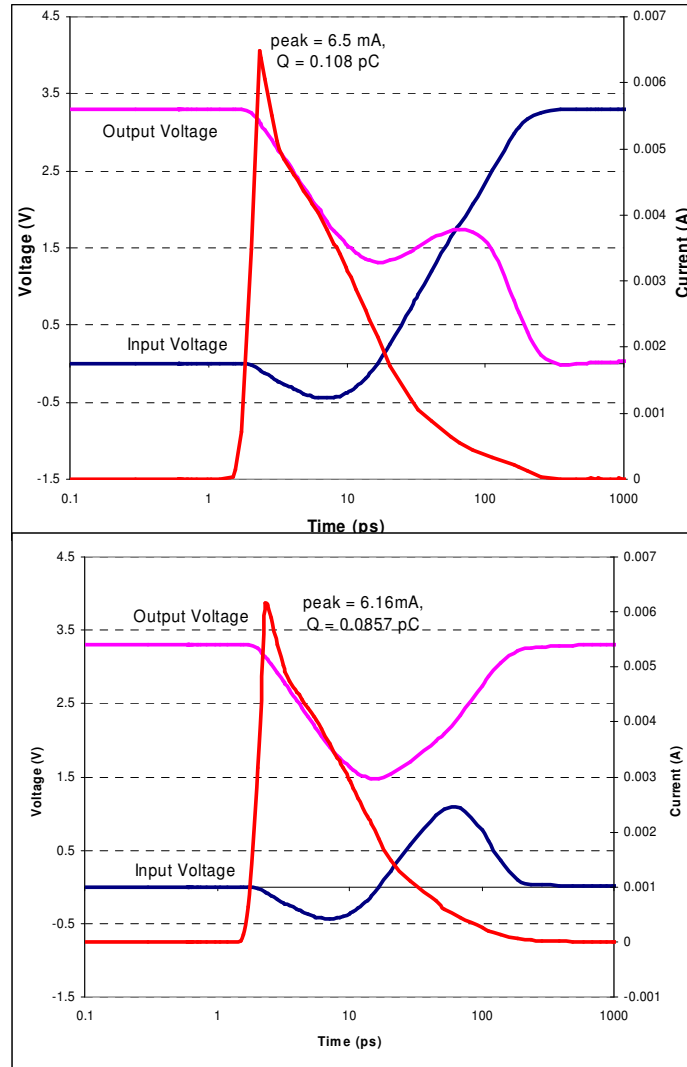


Figure 1: Current vs. Time response of SRAM cell of (Top) slightly higher than critical charge and (Bottom) slightly lower than critical charge. Images taken from TCAD simulations of ion strike on Drain of nFET in 0.5 μm CMOS SRAM cell in this study

The upset mechanism for an SRAM cell is due to the active feedback in the cross-coupled inverter pair that forms a typical SRAM memory cell as shown in Fig. 2. When a particle strikes a sensitive region of the SRAM, transient currents flow through the struck transistor due to the charge collected at the junction⁴. In SRAM cells, four possible nodes are considered sensitive to particle strikes, which correspond to the four transistor drains in the SRAM cell.

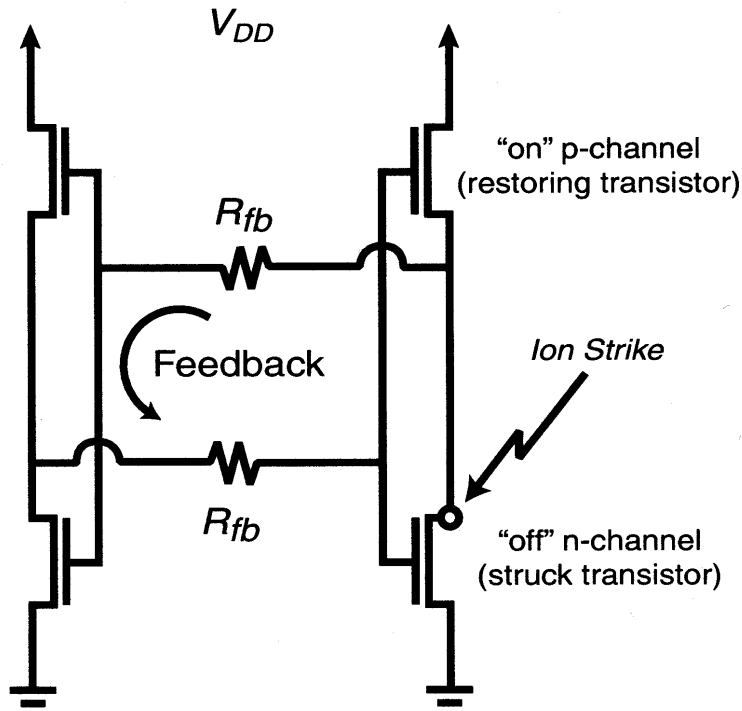


Figure 2: Competition between the feedback process and the recovery process governs the SEU response of SRAM cells⁴

An important distinction is whether the ion strike hits the drain while the MOSFET is operating in the "on" state or "off" state⁵. It has been shown that an ion strike on the drain of the "off" device(s) is considered the most sensitive to particle strikes since the charge deposited deep in the substrate or well can diffuse back into the drain junction⁶.

Additionally, the circuit shown in Fig. 2 uses resistors for feedback as a method to harden the SRAM against radiation effects. The SRAM cell used for this research does not use this approach. In order to quantify the SEU sensitivity for the SRAM, the critical charge, or amount of charge needed to induce an upset as shown in Fig. 1, is measured at the strike region⁷. The amount of critical charge is typically less than the amount collected charge on a struck region which is typically even less than the amount of deposited charge in the same sensitive region.

Critical charge is just one of the useful quantities that provide insight on the internal mechanisms of SEU sensitivity. Though there are many other mechanisms existing in leading edge SiGe BiCMOS process generations that contribute to increased SEU sensitivity, for this study the critical charge will be the dominant mechanism under investigation. These constraints are permissible since the IBM SiGe 5AM 0.5 μm BiCMOS process technology used in this research is larger than leading edge SiGe BiCMOS process generations. In order to visualize the relationship that threshold LET has with certain technology feature sizes, Fig. 3 shows the simulated and experimentally measured SEU thresholds LETs for SRAMs without feedback resistors in three Sandia CMOS technologies⁵.

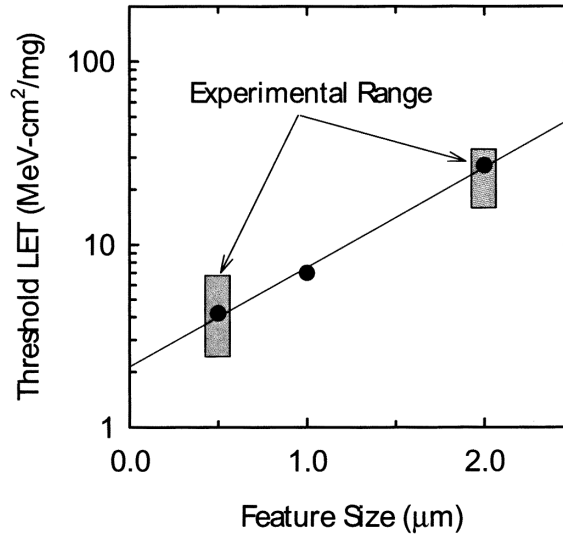


Figure 3: Overall SEU Threshold LET technology trend for three generations of Sandia CMOS SRAMs without feedback resistors⁴. Points represent 3-D mixed-level simulations where as the shaded regions represent the measured range.

This graph shows the range of LETs that can cause upsets for devices with differing feature sizes. As indicated on the graph, feature sizes similar to the process technology under study in this research can typically withstand ion strikes below LETs of 5-7 MeV-cm²/mg. Anything above that threshold can cause SEUs in the SRAM cell unless additional radiation hardening techniques are implemented. An area of great interest, in particular with the process technology in this study, is to see whether operation of the SRAM cell at cold temperatures will cause the cell to flip at LETs below the threshold LET measured at 300K. This decrease in threshold LET could essentially render the radiation hardening techniques ineffective for that range of LETs between the critical LET that caused the flip at that cold temperature and the threshold LET at 300K for which the radiation hardening was intended. To better understand how threshold LETs are determined in SRAMs, Fig. 4 shows the transient response of the drain voltage of an SRAM as it is struck by an incident particle with LET well below, just below, and just above the upset threshold.

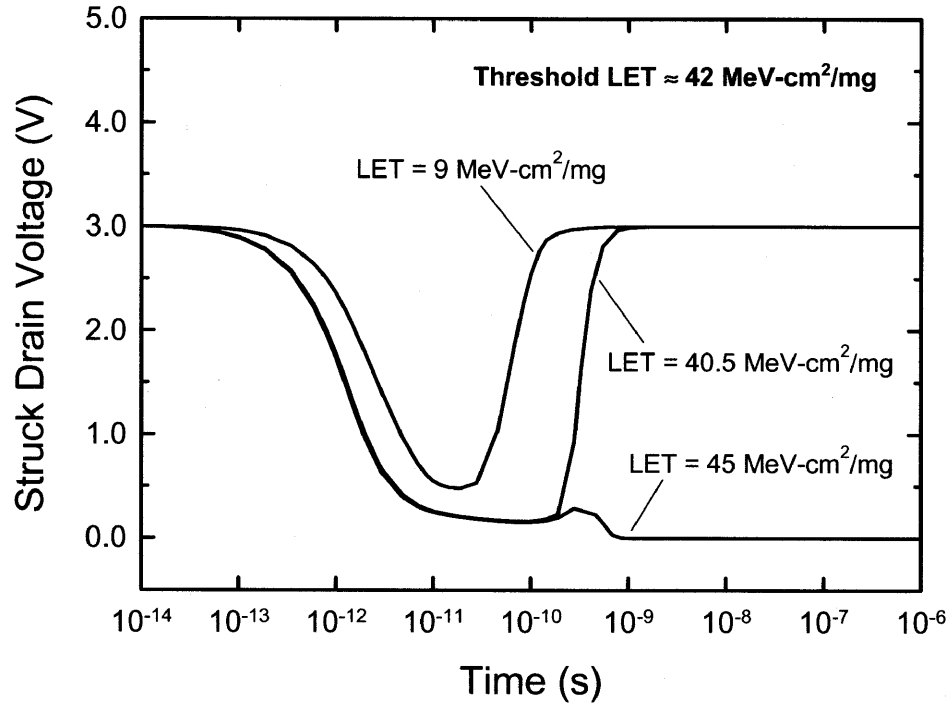


Figure 4: SRAM voltage transient of ion strike on drain with LET well below, just below, and just above the SEU threshold⁴

It can be seen clearly in the graph that the threshold LET is somewhere between 40.5 and 45 MeV-cm²/mg for the hardened cell design. However, it is interesting to see that a particle well below the threshold LET can induce a significant voltage transient on the struck drain. Furthermore, a question of particular importance for this research is whether cold temperatures will exacerbate this voltage transient that could lead to increased sensitivity to SEUs.

Temperature Dependence

Electronics designed for commercial applications are tested to operate in temperature ranges between 0 and 85°C. The standard mil-spec temperature range for electronics can range from -55°C to 125°C. However, special situations can require the operation of these electronics to function above and below these ranges of temperatures. If a system is designed with specific SE error immunity, changes in the temperature can cause the immunity to degrade to where the upset threshold of the device decreases⁸.

In this research, the temperature ranges that are of concern are the cold temperature ranges that extend below the mil-spec temperature ranges. SiGe BiCMOS has shown promise in this environment of cold temperatures. Although there is limited data available on CMOS at cold temperatures, none exist in this technology process. The results of this research could indicate a need for radiation hardening on the SRAM cell in order to withstand SE hits that were thought to be sub-critical at 300K.

Understanding the relationship that temperature has with CMOS devices was essential for hypothesizing what effect cold environments would have on the SRAM cell. Several attributes of CMOS devices are affected by cold temperature operations. The mobilities are shown to have temperature dependence. Fig. 5 shows how the electron and hole mobility are increased at low temperatures⁹. The channel conductance is increased as seen on Fig. 6 as the gate voltage is increased at lower temperatures¹⁰.

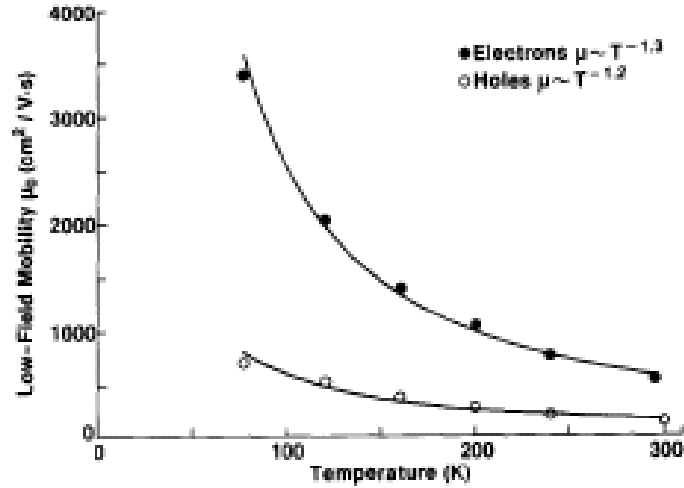


Figure 5: Mobility of electrons and holes are increased as temperature is decreased⁹

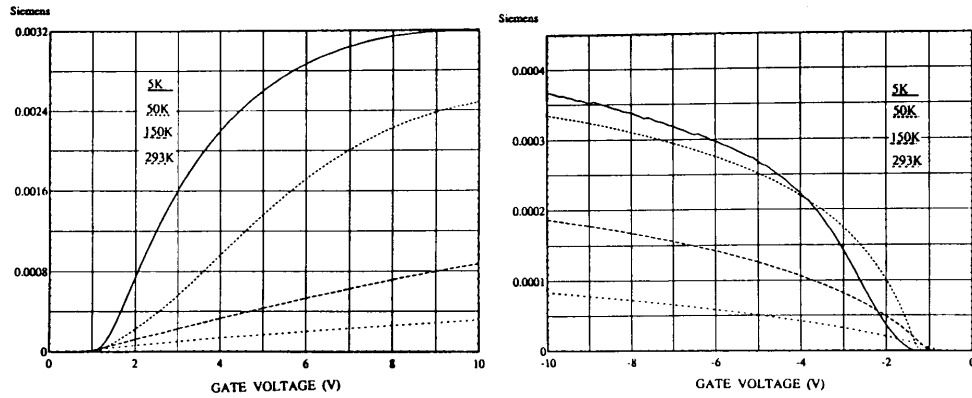


Figure 6: Gate Voltage vs. Channel Transconductance: Effects of temperature on the channel conductance of NMOS (left) and PMOS (right) devices¹⁰

Another effect of decreased temperature in MOSFET's is the change in recombination lifetime. Although past studies have shown that the recombination lifetime will increase as temperature decreases¹¹, there has been conflicting data stating a decrease in recombination lifetime¹². While these temperature effects shown above have been suggested to improve ground level performance of commercial CMOS devices, when these same devices are subjected to the harsh environments of space, where many of these cold temperature ranges exist, these enhancements could lead to degrading effects¹⁵.

The operation of CMOS devices in space environments present challenges factoring in both radiation and temperature effects on circuit performance. Most published works have focused the response of circuits operating at high temperatures^{8,13} and temperatures within the lower limit of the mil-spec temperature range¹⁴ in the space environments showing how charge collection is affected by temperature. It has even been shown that at sub-critical LETs the particle flux can increase the upset cross section of an SRAM as the temperature is decreased below the mil-spec limit. All of this suggests a degradation of performance of CMOS SRAM cells which will lead to an increased sensitivity to SEUs as the temperature is decreased. It will be the purpose of this research to see whether any degradation exists in the CMOS SRAM due to cold temperatures and whether radiation hardening techniques will need to be implemented to maintain an acceptable level of SEU sensitivity guided by the error management system.

IBM 5AM 0.5 BiCMOS Process Technology

The SiGe BiCMOS process technology was chosen for this research because of its inherent TID tolerances and of its ease of use in analog-mixed signal design as well as its superior performance to Silicon Bipolar Junction Transistors (BJTs) at cold temperatures. Though Silicon BJTs are advantageously faster, the degradation at cryogenic temperatures make them unappealing for this application^{15,16,17,18,19,20}. In fact, SiGe HBTs have been shown to have characteristics that fare better than most Silicon BJTs in the cryogenic temperature environment²¹. Given that most foundries prefer to fabricate SiGe HBTs as a BiCMOS process, which includes a Si CMOS portion in the process, this

equates to a large demand in having these CMOS devices function as well as their SiGe HBT counterparts. A cross section of the process technology used in this research that will be used in these cold temperature simulations is shown as Fig. 7.

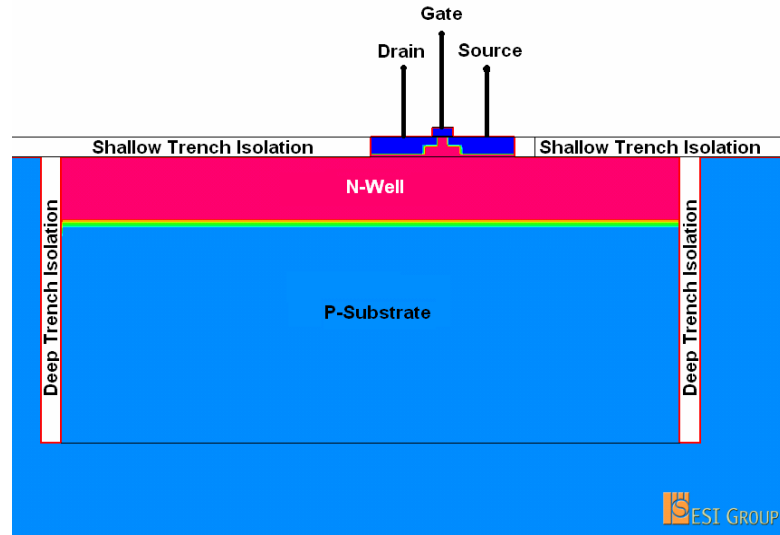


Figure 7: Figure of the CMOS pFET designed in the BiCMOS process. This device was used in this paper

Breaking down the name of this technology is as follows: SiGe refers to the Germanium profile in the Base of the HBT, BiCMOS refers to the duality of the process of HBTs and CMOS devices, and 5AM refers to the five metal layer interconnects with an Analog Metal optional layer on top. This technology offers the advantages of SiGe and lower power consumption compared to silicon bipolar devices as well as higher gain and less noise. Some of the necessary specifications for the IBM SiGe 1 μm BiCMOS 5AM process can be seen as Fig. 8.

Specifications		
SiGe HBTNPNs		
	Small-Signal/Low-Voltage High-Speed Device	High-Power/High-Voltage Low-Noise Device
BV_{ceo}	3.3 V	5.5 V
Gain	100	80
f_t	47 GHz	30 GHz
f_{max}	65 GHz @ $V_{cb} = 1V, V_{be} = 0.72V$	55 GHz @ $V_{cb} = 1V, V_{be} = 0.72V$
V_{early}	65 V	124 V
FETs		
	NFET (W/L = 10/0.5 μm)	PFET (W/L = 10/0.5 μm)
T_{ox}	7.8 nm	7.9 nm
L_{eff}	0.39	0.39
G_{max}	103 mS/mm	180 mS/mm
V_{thn}	0.55 V	0.6 V
R_{ext}	500 Ω - mm	500 Ω - mm
I_{sat}	400 $\mu A/mm$	400 $\mu A/mm$
CAPs		
MOS Cap	1.50 fF/ μm^2	
MIM Cap	0.70 fF/ μm^2	
Diodes		
SD (Schottky)	$V_f = 300\text{ mV}@100\text{ }\mu A$	
PIN	$V_f = 790\text{ mV}@100\text{ }\mu A$	
VARactor	1.4 fF/ $\mu m @ 0V$ $V_f = 810\text{ mV}@100\text{ }\mu A$	
ESD	2000 V HBM	
Spiral Inductors* (examples)		
4Turn:	Q(2 GHz) = 7.5, 4.2 nH	
6Turn:	Q(1 GHz) = 5.8, 9.8 nH	
8Turn:	Q(1 GHz) = 5.2, 16.6 nH	

Figure 8: Physical specifications for the IBM SiGe BiCMOS 5AM process²²

For the purposes of this research, since an SRAM cell was simulated, only the CMOS portion of this process was examined. Furthermore, since this technology is matured and it is considerably larger than the leading edge generation, the focus of the simulations was put on the temperature dependency of SEU sensitivity.

CHAPTER III

THE CFDRC AND ESI GROUP SOFTWARE BUNDLE

Introduction

The current software available for mixed-mode simulations at Vanderbilt is the Dessis software. Unfortunately, Dessis lacks some of the ease of use and compatibility required for this research. Since Dessis can not take the PDKs directly from the devices, a painstaking process of extracting all the scaling, dependencies, etc, from the PDKs for each process technology is required. On the other hand, Cadence's Spectre software can implement the devices for mixed-mode directly from the PDKs. Therefore, there was a desire to take advantage of this tool's feature. CFD Research Corporation (CFDRC) created a tool called MixCAD that seamlessly coupled the Spectre circuit simulators with their NanoTCAD solvers. It was therefore decided to implement the 3D TCAD devices built in this research in the CFDRC software bundle in order to utilize this new feature.

The entire CFDRC and ESI product package consists of multi-physics software as well as pre- and post-processing tools²³. This software bundle provided an ease of use and compatibility between the compact and TCAD models. Lynguent Technologies provided the model parameters for the compact models, in MEXTRAM and BSIM, necessary to simulate the circuits at cold temperatures. The CFDRC and ESI software bundle allowed seamless interfacing between the compact models of MEXTRAM and BSIM, in Cadence Spectre, to the NanoTCAD solvers. Not only was this convenient in terms of compatibility, but the cold temperature models offered by CFDRC and ESI

allowed for a better convergence for the devices operating in those temperature ranges. The following tools are a part of the CFD and ESI package: CFD-Micromesh, CFD-VIEW, CFD-ACE-GUI, NanoTCAD, SimManager, and MixCAD. The following sections will detail how the software bundles were used to build the TCAD nFET and pFET. The ability to view and analyze all the images created, shown as various figures below, by the CFD and ESI software packages is possible through the program CFD-VIEW.

CFD-Micromesh

CFD-Micromesh is an automated tool used for three-dimensional geometry building and mesh generation from layouts²⁴. A screenshot of the software can be seen below as Fig. 9.

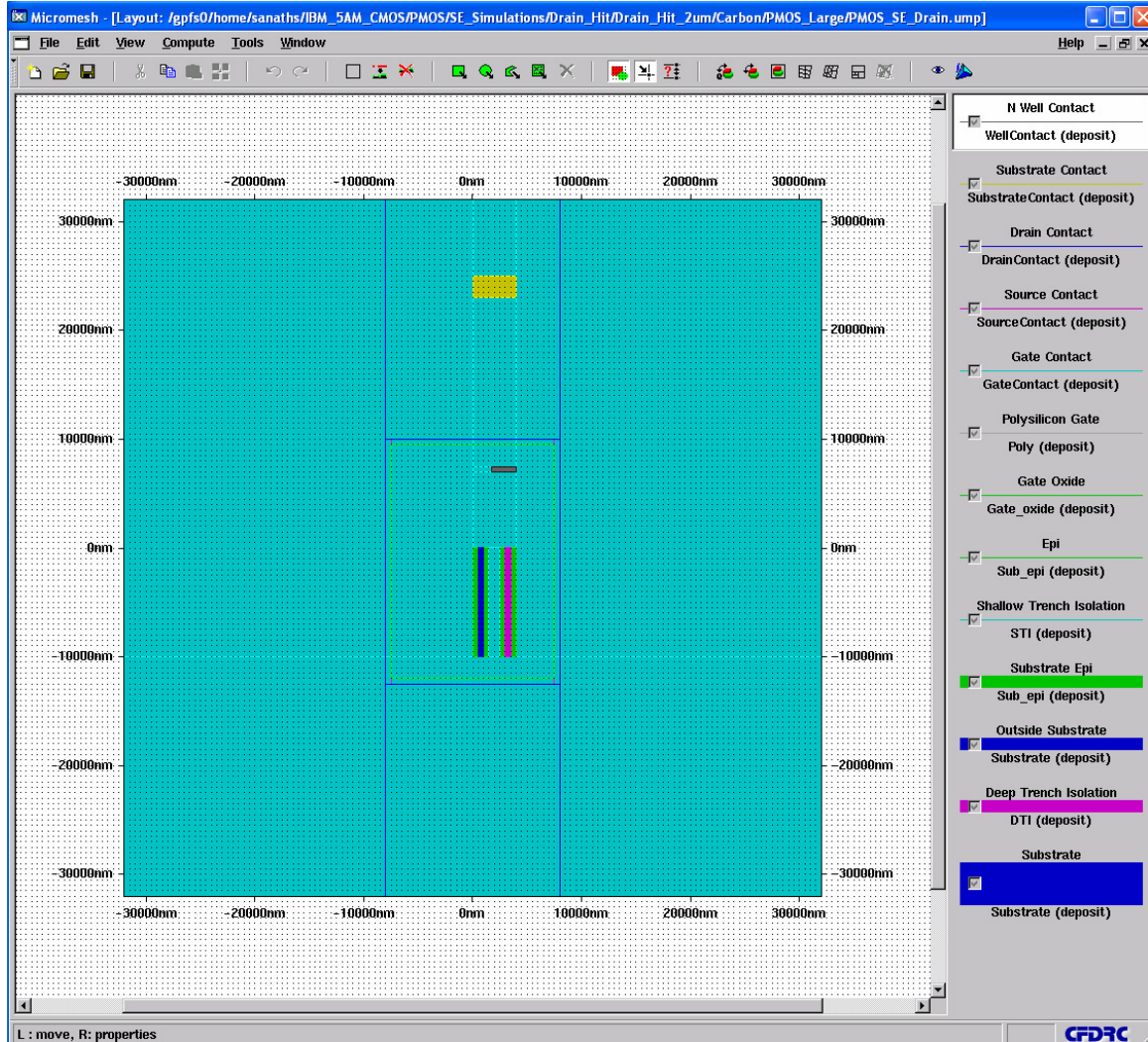


Figure 9: Screenshot of CFD-Micromesh

The list of colored blocks on the right side indicates the different levels of physical blocks that make up the structure. The software builds the devices based on volumetric pixels (voxels) which are used to create the solid device shapes. CFD-Micromesh uses smoothing techniques on these voxels in order to render the 3D mesh. CFD-Micromesh

allows for the voxel resolution to be refined further by implementing refinement files which specify segments of the physical device to be meshed into smaller increments in order to keep the device model accuracy consistent. Upon completing the physical specifications and mesh refinements, the software outputs a Data Transfer Facility (DTF) file which is universally adapted into all of the software packages for further manipulation and analysis of the devices.

At this stage of development, the geometries have no electrical or doping characteristics. They are considered to be 3D blocks of varying sizes. In order to add doping profiles, define regions, and attribute other types of characteristics, the DTF file needs to be edited in the software package CFD-ACE-GUI.

CFD-ACE-GUI

In order to specify the devices electrical characteristics to perform the appropriate functions, the program called CFD-ACE-GUI is used to set up the simulation. CFD-ACE is considered a multi-physics program, meaning it can perform coupled simulations of fluid, thermal, chemical, biological, electrical, and mechanical phenomena²⁵. For the purposes of this research, only the electrical and thermal aspects of the software were utilized. Fig. 10 shows a screenshot of the program.

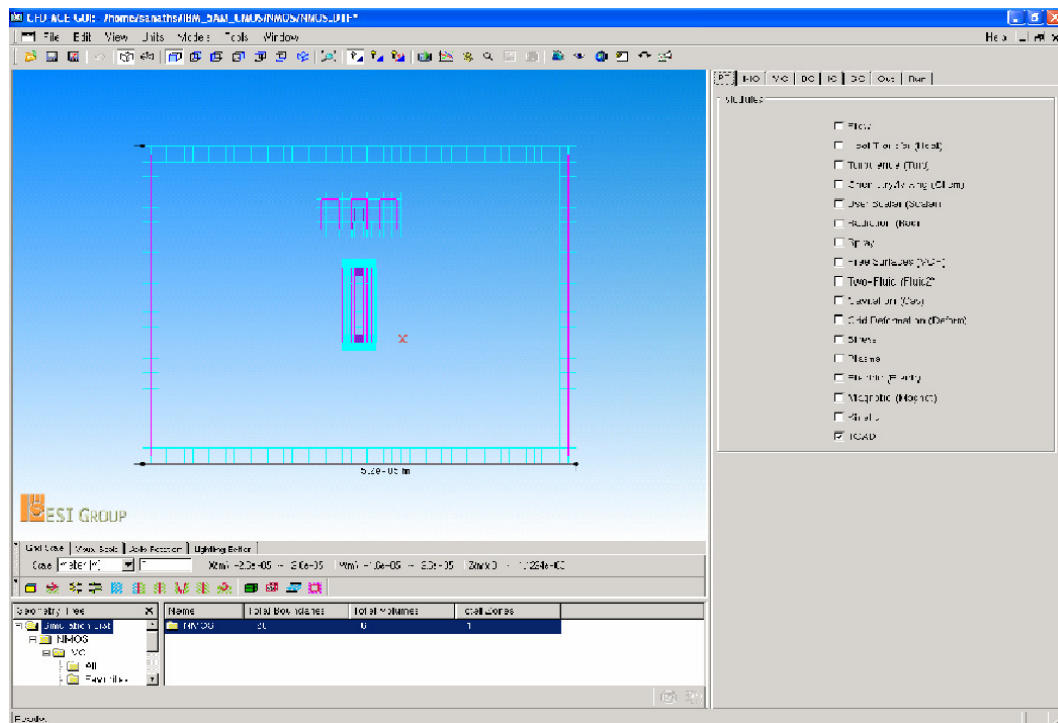


Figure 10: Screenshot of CFD-ACE Graphical User Interface

The tabs on the upper right allowed for an easy transition between steps for specifying regions and functions of the devices. Since the program is a Graphical User Interface (GUI), all the intermediate steps of specifying the initial and steady-state conditions are visually friendly.

At this point, the doping profile is incorporated into the DTF file and the initial and steady-state conditions are specified for the devices. Additionally, the actual solving of the initial and steady-state conditions is performed by the CFD solver, NanoTCAD. The CFD-ACE program allows control of the solver and the output displays. Adjustment of the controls in CFD-ACE can make NanoTCAD perform smoother and quicker simulations.

NanoTCAD

NanoTCAD is the solver program of the CFD and ESI software package. It uses the finite volume numerical method to solve fundamental equations of carrier continuity coupled to the Poisson's equations²⁶. Once the simulation is set up specifying the volume and boundary conditions as well as the solver controls and output displays using the CFD-ACE program, the DTF file, containing the 3D geometry and meshing, is submitted to the solver and the device is given the appropriate characteristics. The solver takes into consideration fundamental current and voltage equations in order to simulate the device. NanoTCAD solver was used to perform DC voltage sweeps in order to calibrate the TCAD nFET and pFET to the PDKs for the IBM SiGe 5AM nFET and pFET. DC voltage sweeps are specified in a program SimManager, a screenshot can be seen below as Fig. 11, and subsequently are submitted to the solver.

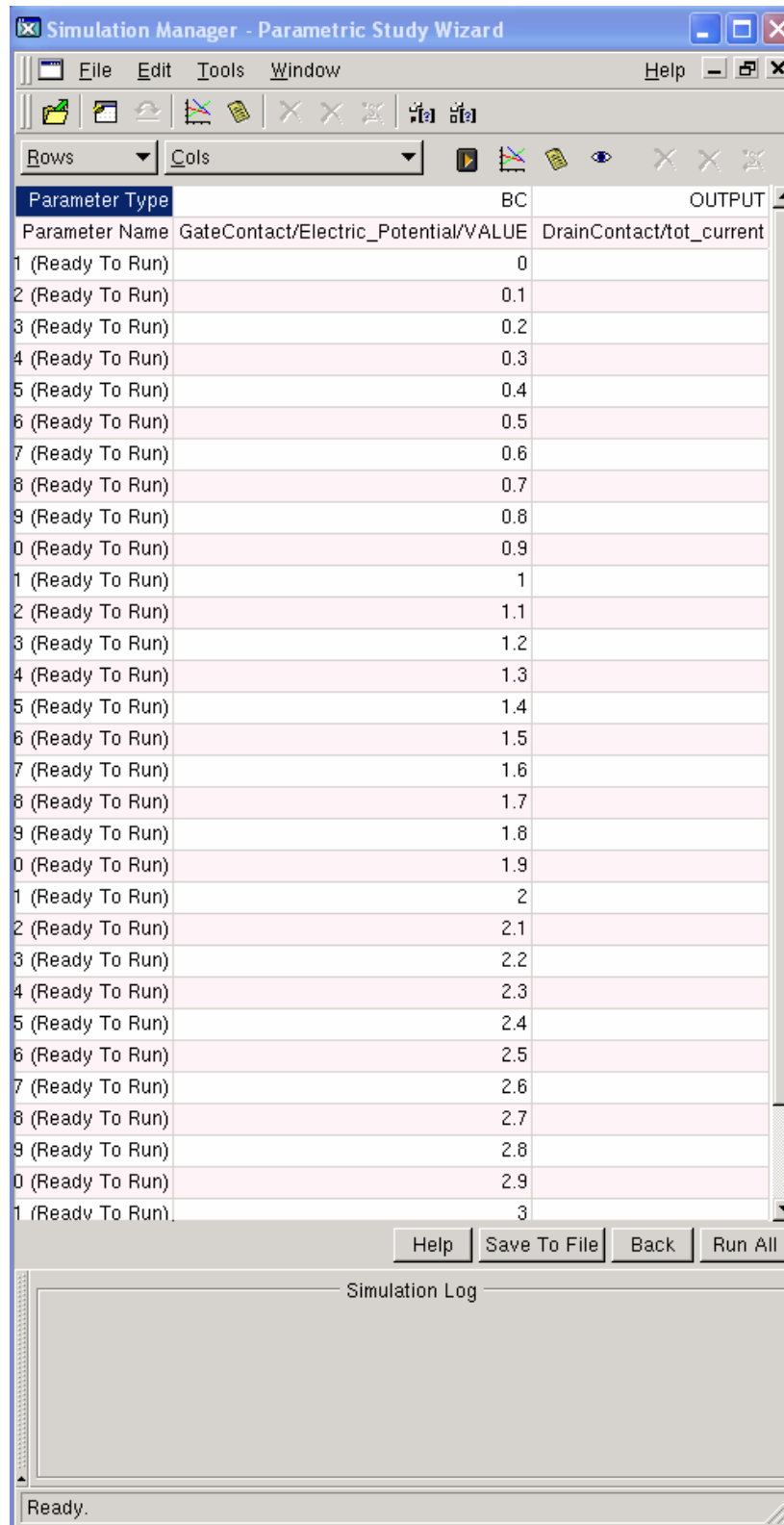


Figure 11: Screenshot of SimManager used to run DC voltage sweeps.

The solver was used to perform the transient simulations that were used to simulate an ion strike in order to calibrate the TCAD nFET and pFET to the charge collection data of the IBM SiGe 5AM 0.5 μm devices. The details, results, and comparisons of these simulations can be found in Chapter IV.

MixCAD

The MixCAD software is a newly developed mixed-mode program that allows a direct coupling between TCAD and Spice simulations. This allows for the advantages of both types of simulations; the speed of Spice (Spectre) with the physical insight of TCAD (NanoTCAD). Spectre is a general purpose electronic circuit simulation program offered by Cadence Design Systems²⁶. It uses a Newton-Raphson algorithm for every numerical solution of the circuit equations. The MixCAD software acts as a coupling mechanism between the solvers NanoTCAD and Spectre. The flow chart shown as Fig. 12 demonstrates how the information between the two programs is coupled²⁷.

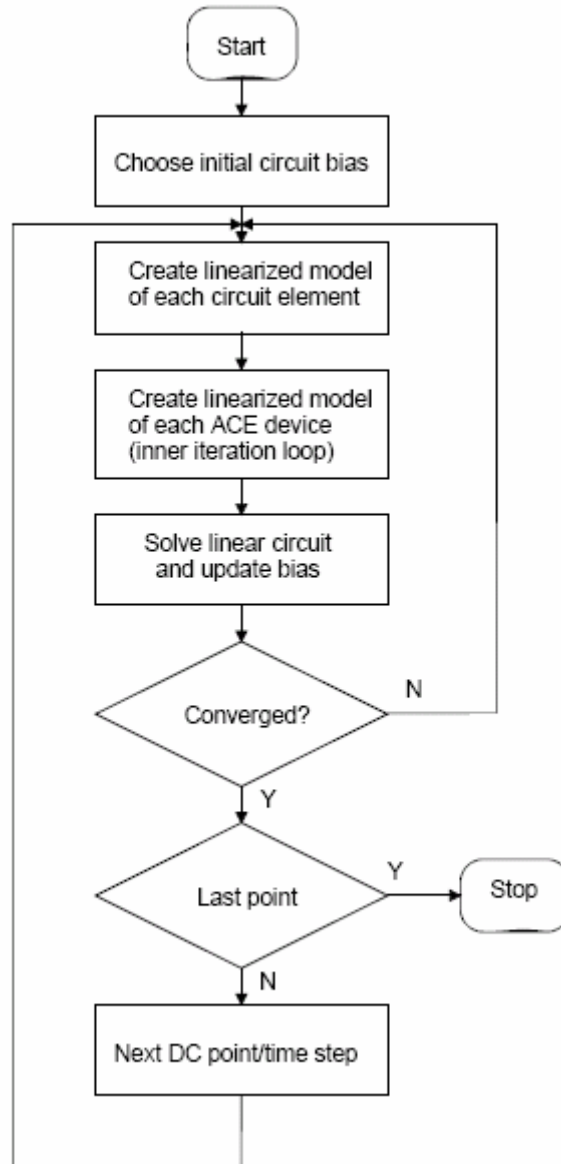


Figure 12: Flowchart showing the coupling and flow of information between NanoTCAD and Spectre²⁷.

The MixCAD simulation process starts with Spectre reading in the libraries and netlists of the NanoTCAD device. For every DC operating point, a Newton-Raphson iteration loop is run until convergence. At the boundaries of the Spectre devices, the applied voltage, for every iteration, is calculated and transferred to the NanoTCAD

device. The currents are calculated in NanoTCAD and are fed back to the circuit simulator, Spectre. The diagram below shows this process.

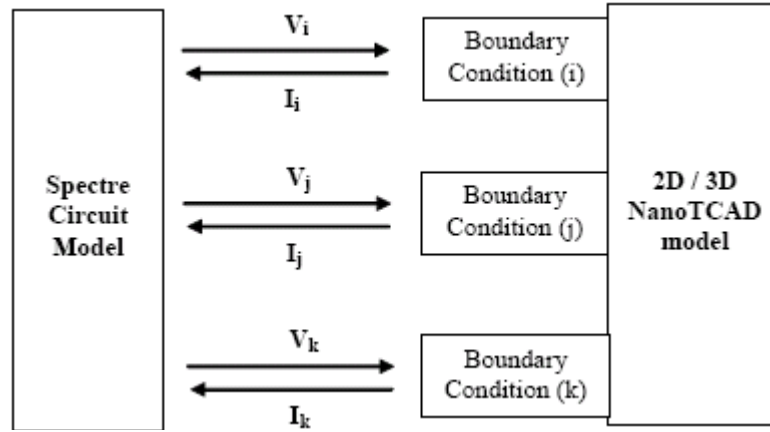


Figure 13: Diagram of the information exchanges between the Spectre and NanoTCAD solvers²⁷

These simulations were used to run mixed-mode simulations on the SRAM cell containing the IBM SiGe 5AM nFET and pFET devices. The simulations were used to determine the threshold LET of the SRAM cell and observe the temperature dependence. The set up, results and analysis of these simulations can be seen in Chapter IV.

CHAPTER IV

CHARGE COLLECTION COMPARISON

Introduction

The calibration of the TCAD nFET and pFET to the IBM SiGe 5AM 0.5 μm nFET and pFET was achieved in multiple steps. First, the TCAD devices were calibrated to PDKs, provided by IBM, of the 10 μm x 1 μm (W/L) devices created in the IBM SiGe 5AM BiCMOS process technology. The dimensions of 10 μm x 1 μm were used because the charge collection data²⁸ were IBM SiGe 5AM 10 μm x 1 μm devices, shown as Figs. 14 and 15. The charge collection data was obtained by bombarding the nFET and pFET with ions of both Carbon and Oxygen with energies of 36 MeV at hit locations covering the devices entirely.

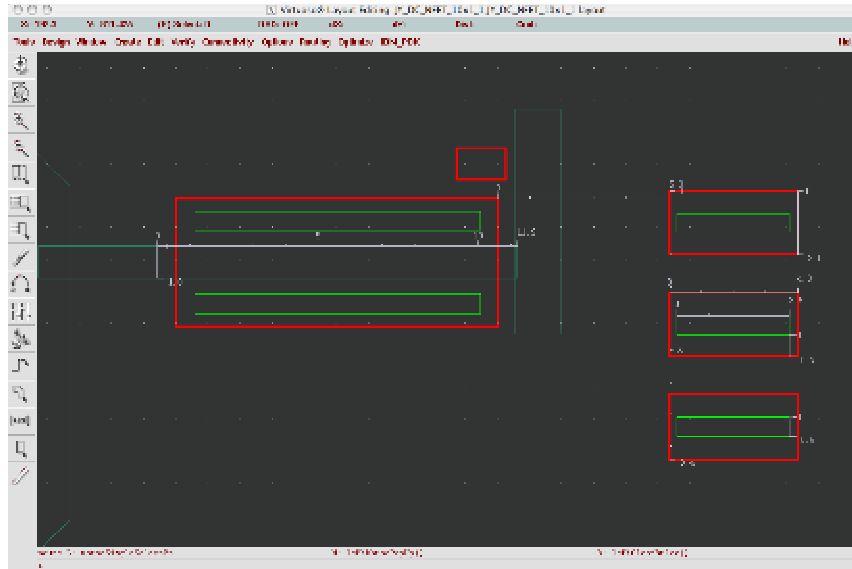


Figure 14: Schematic Layout of the IBM SiGe 5AM 10 μm x 1 μm nFET device

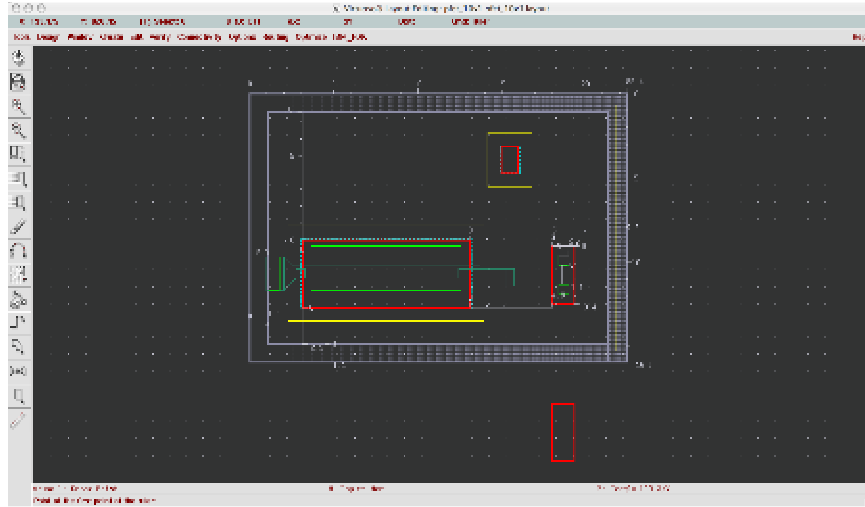


Figure 15: Schematic Layout of the IBM SiGe 5AM 10 μm x 1 μm pFET device

The next step was to run SE simulations on the TCAD nFET and pFET to see how well the charge collection data obtained by simulation would compare to the measured data. This was done in order to ensure that the results of the SRAM cell simulations, results of which can be seen in chapter V, were consistent with the IBM SiGe 5AM 0.5 μm BiCMOS process technology.

The data presented in this chapter shows that the simulations are consistent with the IBM PDKs and the experimental charge collection data. Therefore, the TCAD SRAM cell, built in Chapter V, is considered a proper SRAM cell fabricated in the IBM SiGe 5AM 0.5 μm process technology.

IV Characteristic curve comparisons

Simulation Setup

The 3D geometries of the TCAD nFET and pFET were built using CFD-Micromesh. Figs. 16 and 17 show the 3D model blocks which make up the physical regions of the nFET and pFET, respectively.

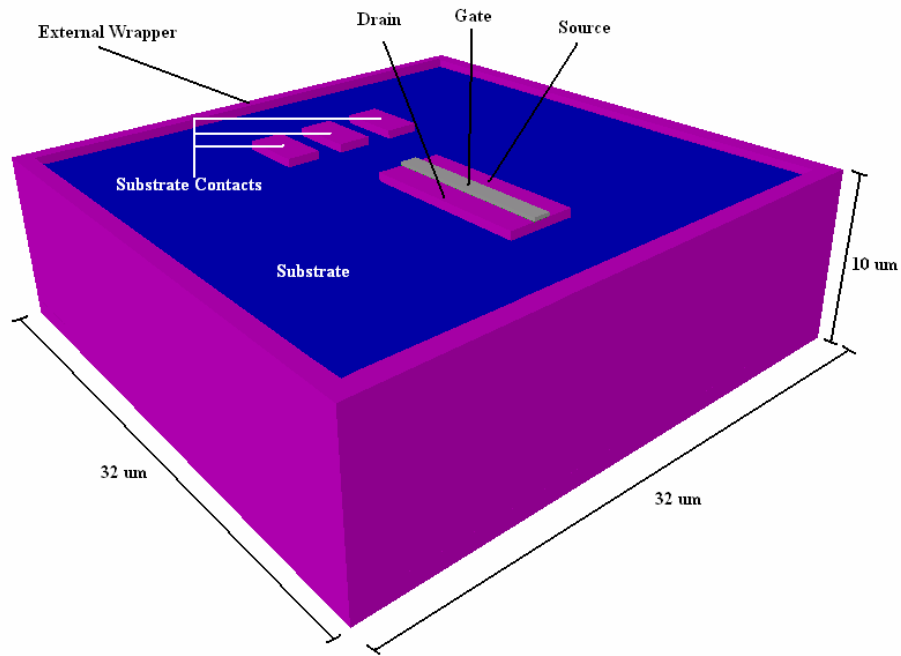


Figure 16: 3D image of physical regions of the TCAD nFET

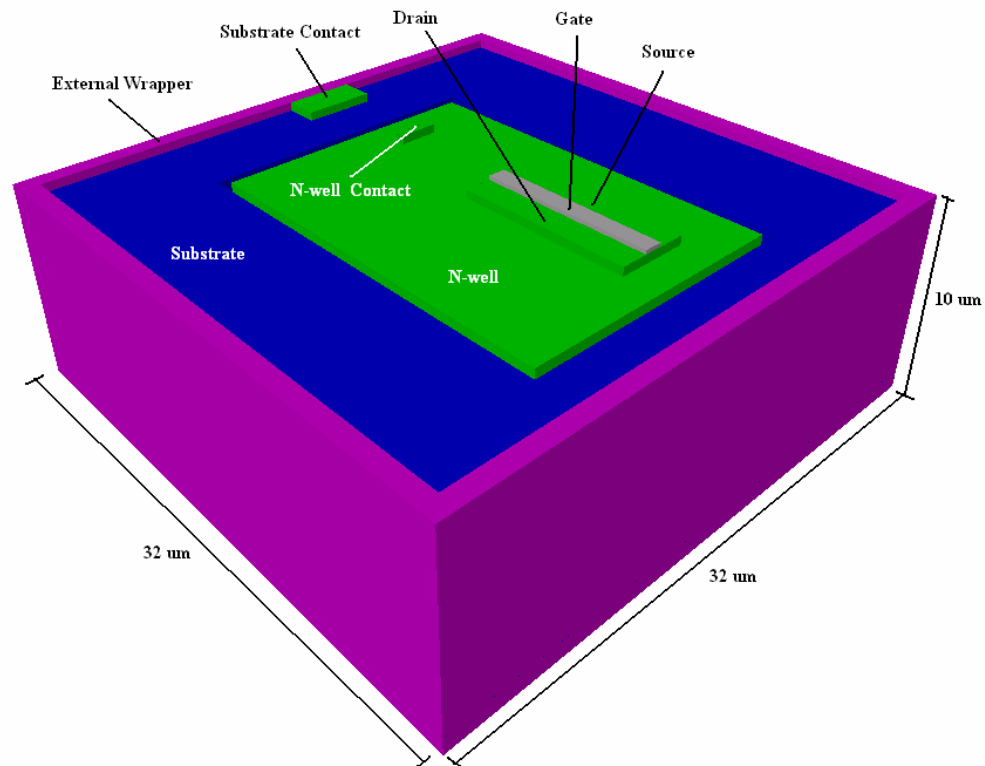


Figure 17: 3D image of physical regions of the TCAD pFET

The TCAD nFET and pFET geometries were then meshed and refined using the process described in the previous chapter. Figs. 18 and 19 below shows the 3D geometry and meshing that were used for the I-V characteristic curve comparisons for the TCAD nFET and pFET, respectively.

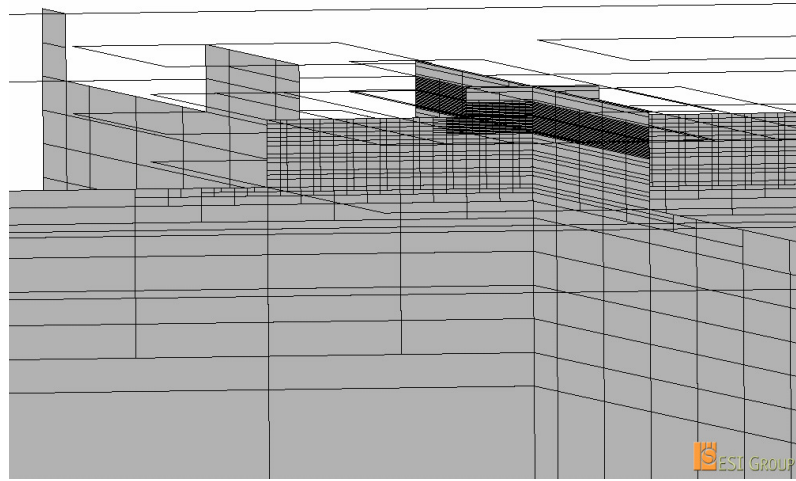


Figure 18: Cross sections in the X and Y directions show the geometry and meshing of the nFET

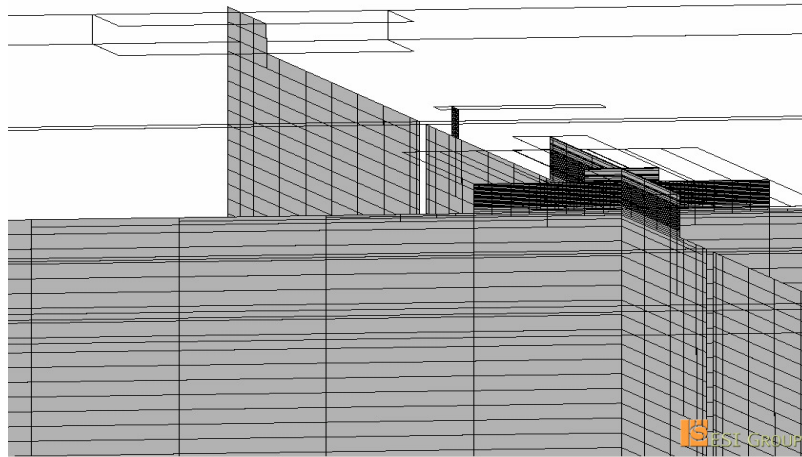


Figure 19: Cross sections in the X and Y directions show the geometry and meshing of the pFET

As can be seen in the figures, the meshing was relatively loose around the substrate and progressively got tighter towards the channels of the two devices. It was important to have the correct amount of refinement as to avoid any dependency issues that could be related to a poorly defined mesh. Additionally, a mesh that is refined too much can take

up an unnecessary amount of time and resources. The related refinement commands can be found in the Appendix.

Once a suitable 3D geometry with an acceptable amount of meshing was created, the device was given the appropriate electrical characteristics using CFD-ACE. Certain regions of the physical models were given attributes similar to semiconductor materials. The attributes were defined in .doping files which specified the regions of the device. The doping profiles of the TCAD nFET and pFET can be seen below as Figs. 20, 21, 22 and 23, respectively. The cut lines in the X and Y directions show the doping concentration gradients between the regions of the device. The doping commands can be found in the Appendix.

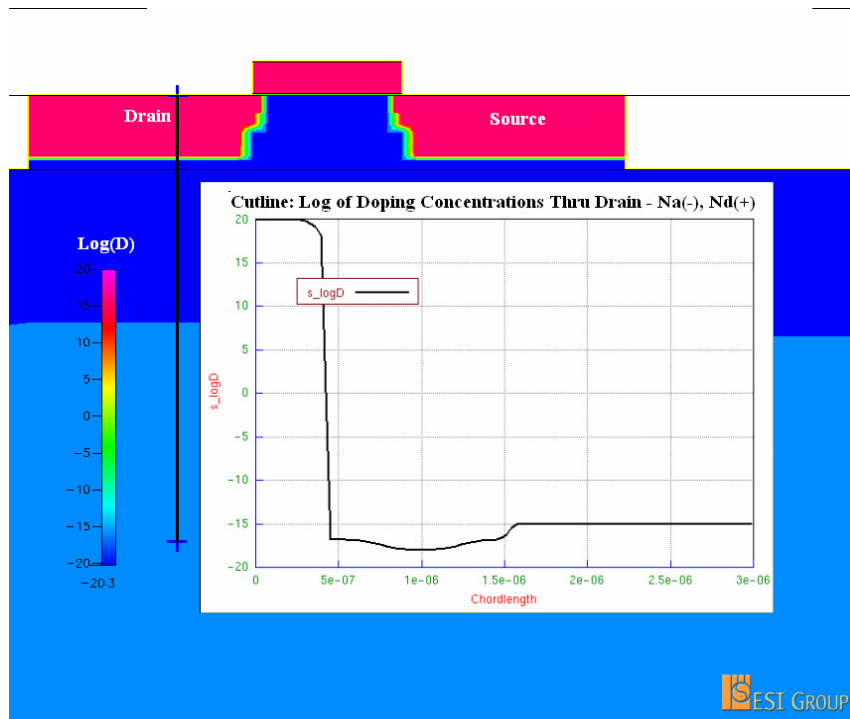


Figure 20: The graph superimposed in this image shows the doping concentration gradient in the Z direction from the contact of the Drain to the Substrate of the nFET.

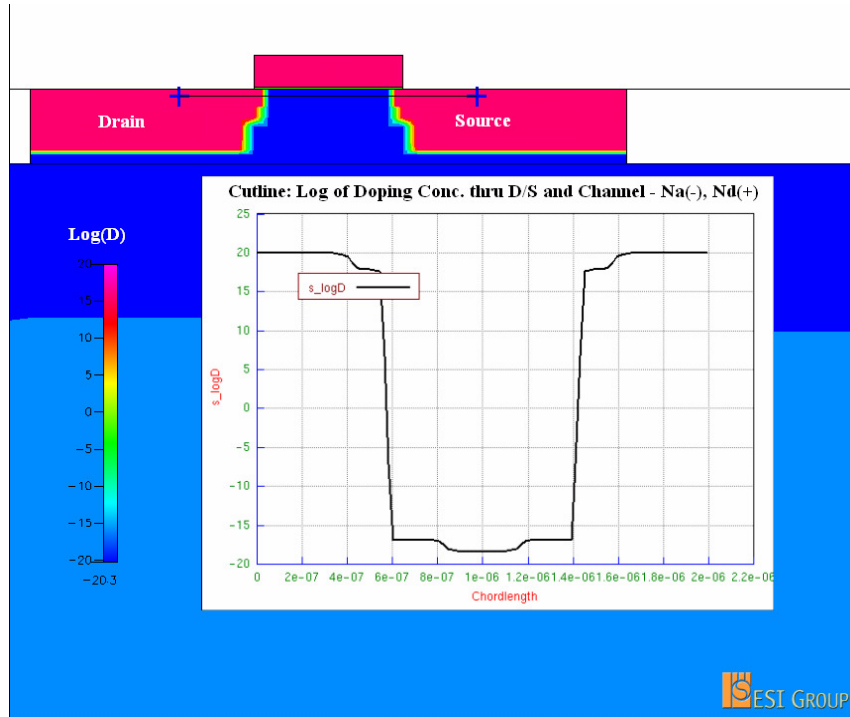


Figure 21: The graph superimposed in this image shows doping concentration gradient in the X direction from the Drain thru the channel to the Source of the nFET

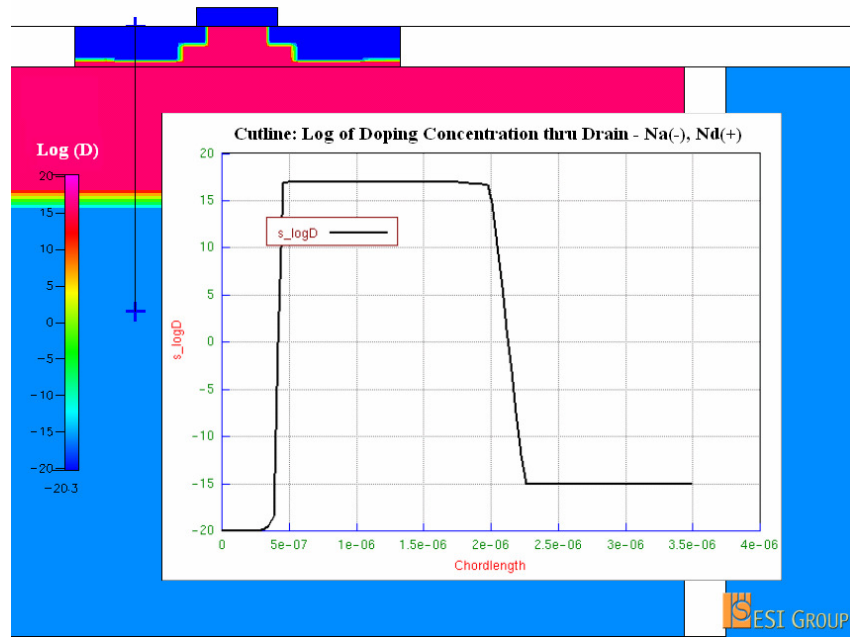


Figure 22: The graph superimposed in this image shows the doping concentration gradient in the Z direction from the contact of the Drain to the Substrate of the pFET

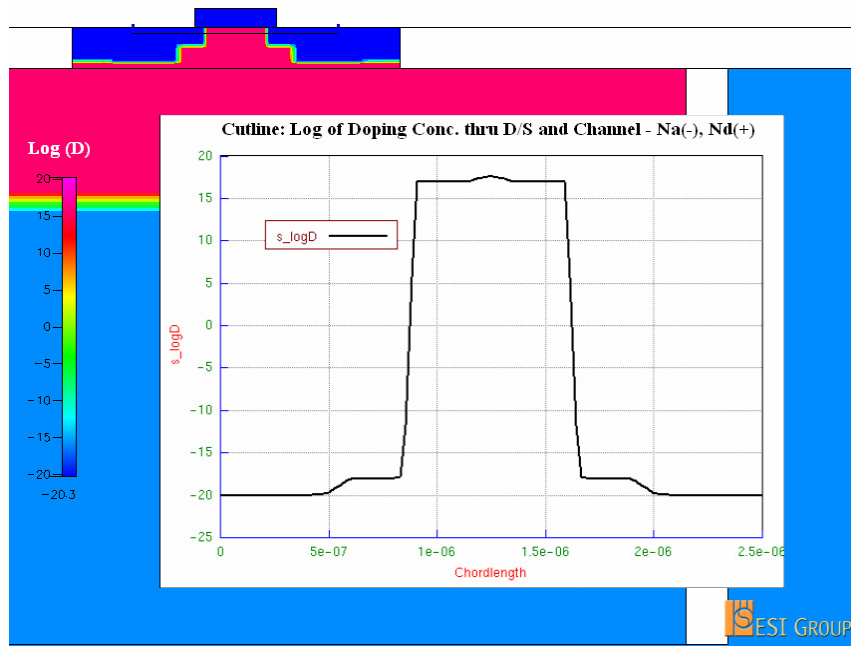


Figure 23: The graph superimposed in this image shows the doping concentration gradient in the X direction from the Drain thru the channel to the source of the pFET.

A few things to notice in these profiles, a V_t implant was used in both the nFET and pFET in order to achieve the correct threshold voltage for the I-V curves. The wells of both devices gradually decrease into the substrate region. Ultimately, these profiles were determined through extensive I-V characteristic curve generations and comparisons with the PDKs for the IBM SiGe 5AM 0.5 μm nFET and pFET devices.

Results

Several DC sweeps were performed in NanoTCAD, in order to justify the use of the doping profiles shown above. A total of five DC sweeps were performed. Two sweeps kept the Drain voltage constant ($V_d = 0.1\text{V}$ and $V_d = 3.3\text{V}$) while varying the Gate voltage from ground to VDD and three sweeps kept the Gate voltage constant ($V_g =$

1.15V, $V_g = 2.376V$, and $V_g = 3.3V$) while varying the Drain voltage from ground to VDD. The results of these DC sweeps and the comparison to the PDKs can be seen below as Figs. 24, 25, 26 and 27.

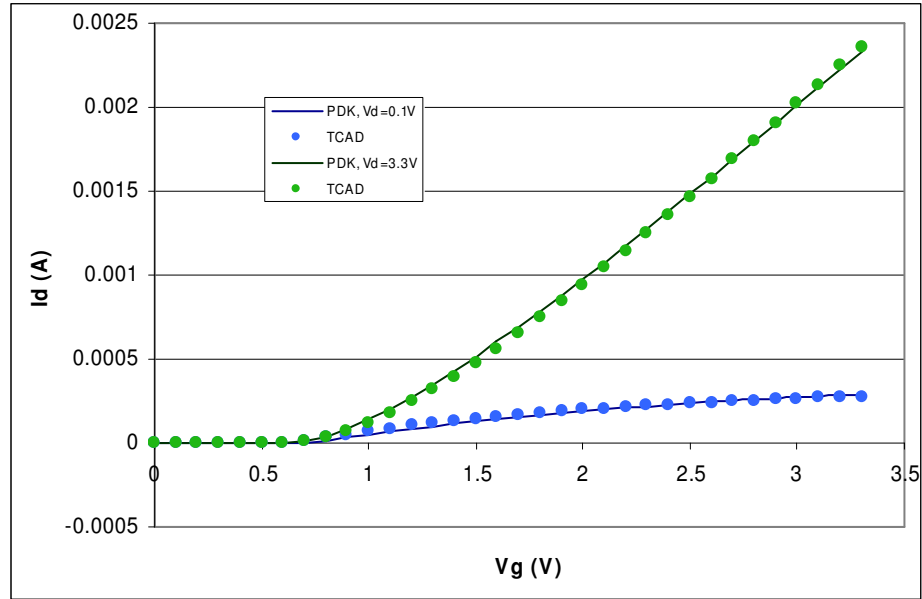


Figure 24: IBM SiGe 0.5 μm nFET I_d vs. V_g Characteristic Curves calibrated to PDK

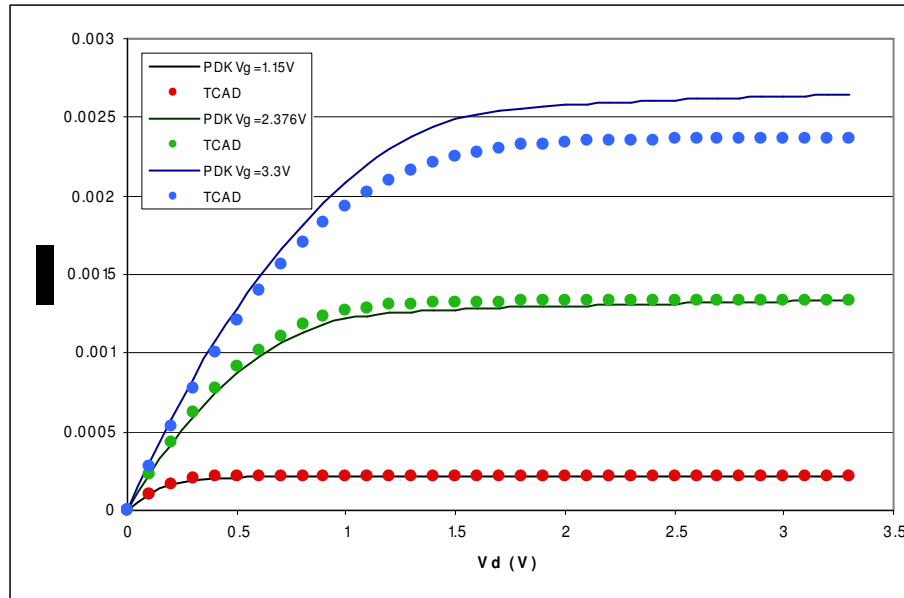


Figure 25: IBM SiGe 0.5 μm nFET I_d vs. V_d Characteristic Curves calibrated to PDK

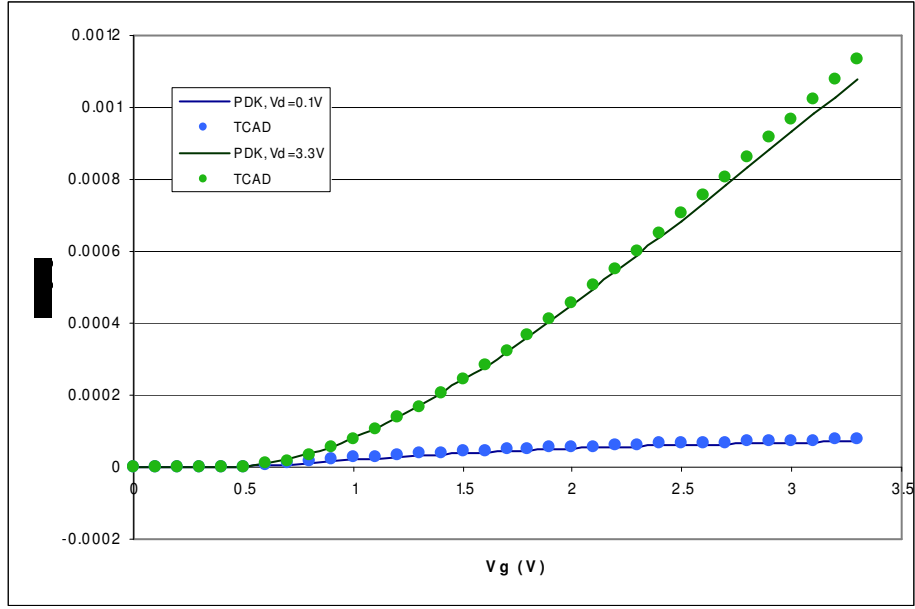


Figure 26: IBM SiGe 0.5 μm pFET I_d vs. V_g Characteristic Curves calibrated to PDK

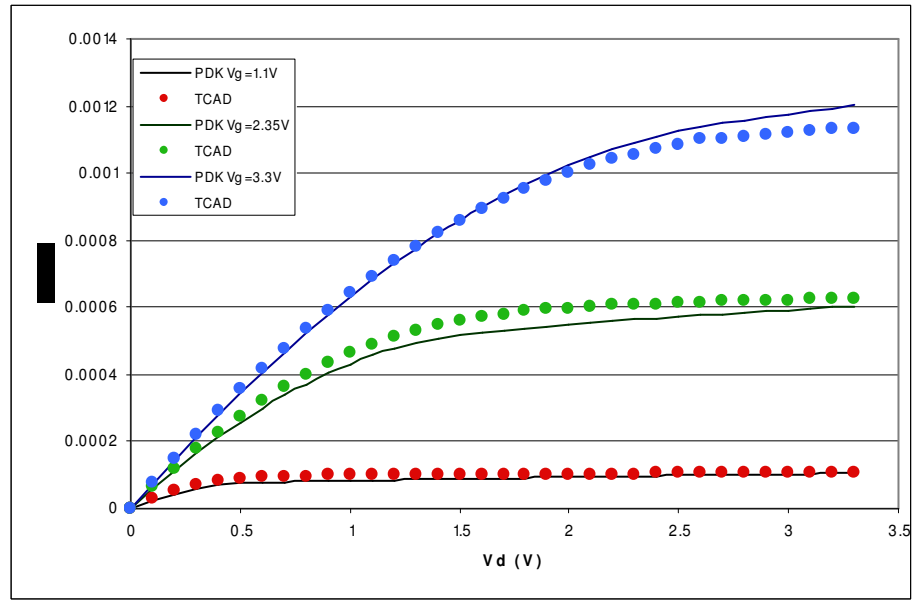


Figure 27: IBM SiGe 0.5 μm pFET I_d vs. V_d Characteristic Curves calibrated to PDK

The results for both the nFET and pFET are within a 10% deviation of the PDKs, which was determined to be an acceptable difference for the purposes of this research. This was further justified when these devices were simulated with ion strikes and

compared to the charge collection data obtained by Jonathan Pellish. Details of the charge collection calibration can be found in the following section.

SEE In IBM SiGe BiCMOS 5AM nFET and pFET

There were two types of physical devices that could be used to perform SEE simulations. One of the devices is a device with large boundary regions, shown as Figs. 28 and 29.

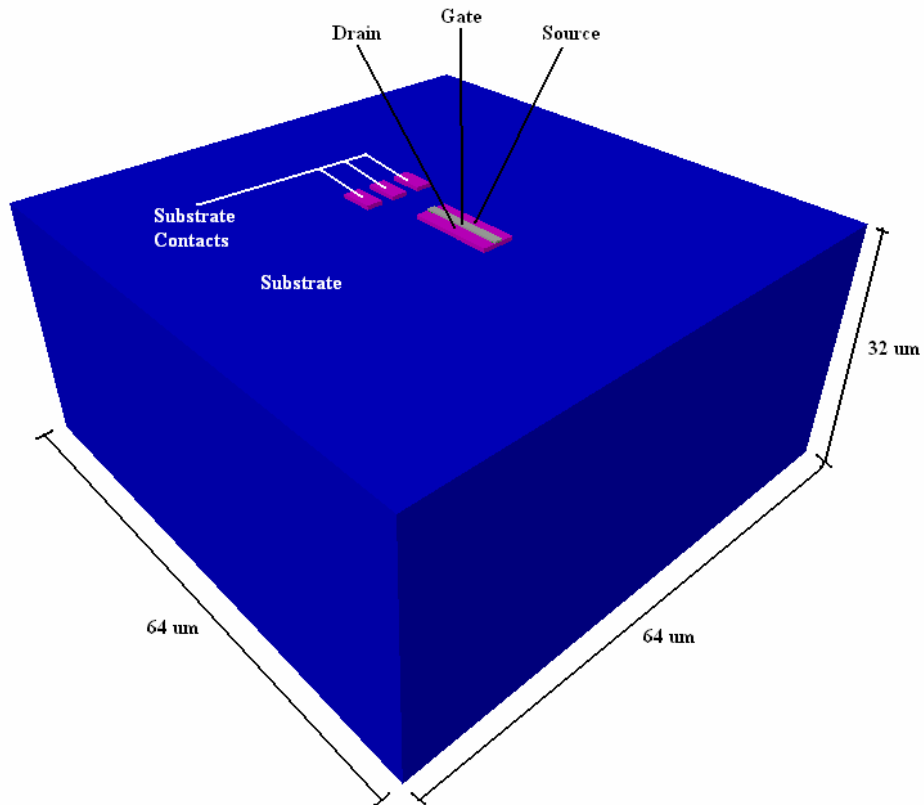


Figure 28: 3D TCAD nFET with dimensions $64\ \mu\text{m} \times 64\ \mu\text{m} \times 32\ \mu\text{m}$ (X-Y-Z) and no wrapper layer

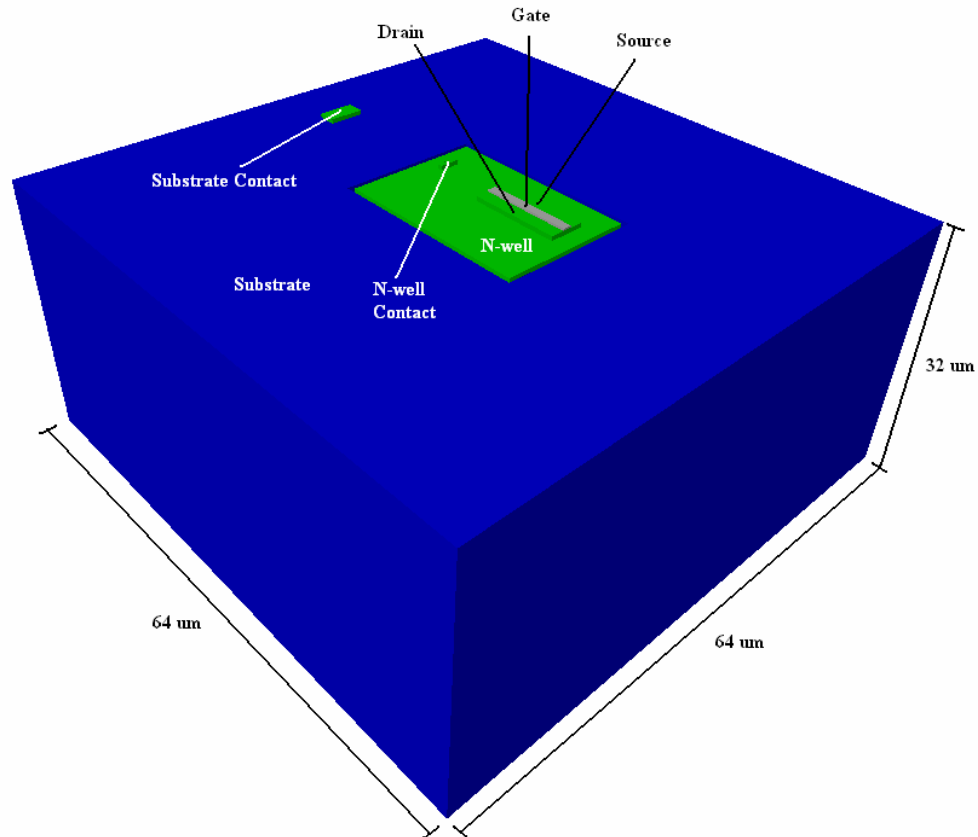


Figure 29: 3D TCAD pFET with dimensions $64\ \mu\text{m} \times 64\ \mu\text{m} \times 32\ \mu\text{m}$ (X-Y-Z) and no wrapping layer

This allows the charge to spread to a reasonable distance away from the device without having to worry about reflection off the boundaries. Devices with smaller physical boundaries have the effect of reflecting charge off the boundaries and back into the device. This leads to an incorrect amount of charge collected in the actual device. Although these devices can be more accurate, the size of these devices creates more meshing points and subsequently more computing resources to render the boundary solutions.

The other type of device implements a wrapper layer around the device with characteristics similar to lower lifetime, shown as Figs. 30 and 31.

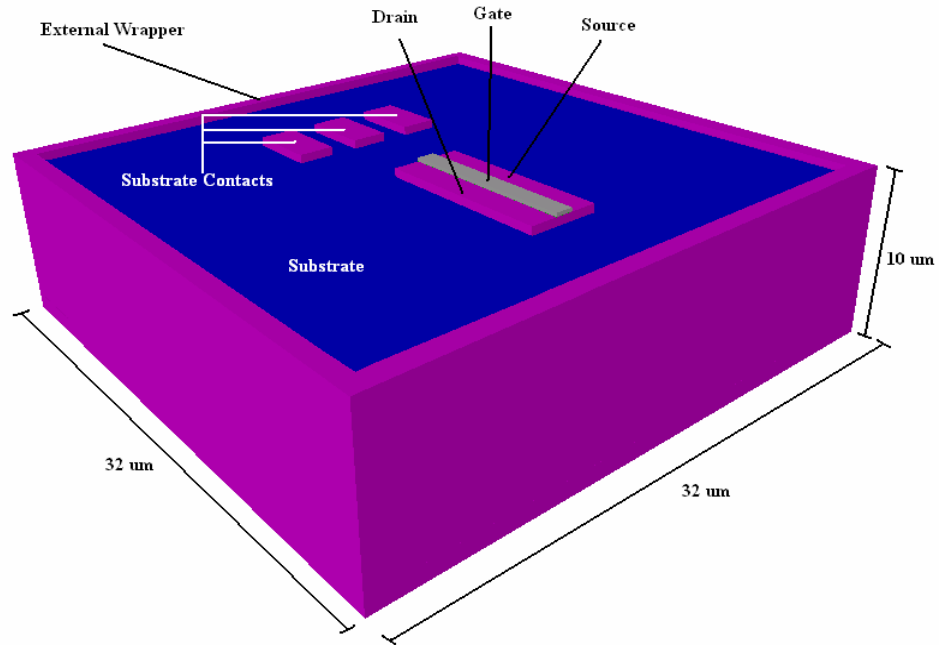


Figure 30: 3D TCAD nFET with dimensions 32 μm x 32 μm x 10 μm (X-Y-Z) including wrapping layer

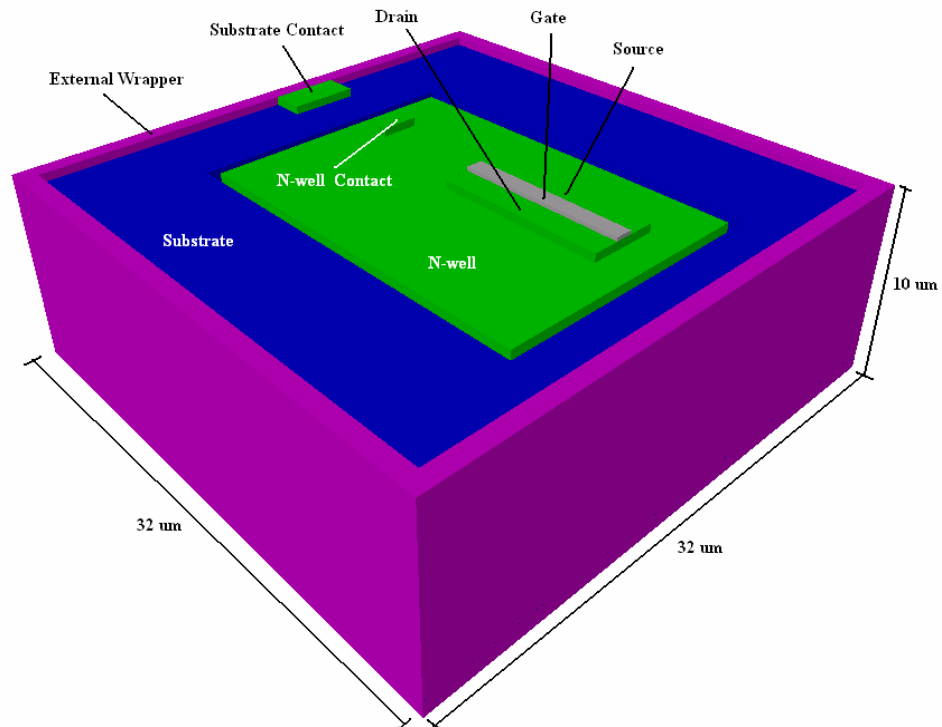


Figure 31: 3D TCAD pFET with dimensions 32 μm x 32 μm x 10 μm (X-Y-Z) including wrapping layer

This takes into account the boundary around the device and essentially acts as a sink collecting the charge which prevents it from reflecting back into the device. This is done by having the lifetime of the holes and electrons in these wrapper regions to be much lower than the substrate region. Therefore, recombination takes place faster in this region than in the substrate of the devices. Since these types of devices are smaller, the computation time is much faster than the larger devices.

Both of these devices were simulated with an ion strike with $LET = 3.4 \text{ MeV-cm}^2/\text{mg}$, similar to a Carbon ion, and the subsequent collected charge was compared. Figs. 32 and 33 show the comparisons for the nFET while Figs. 34 and 35 show the comparisons for the pFET.

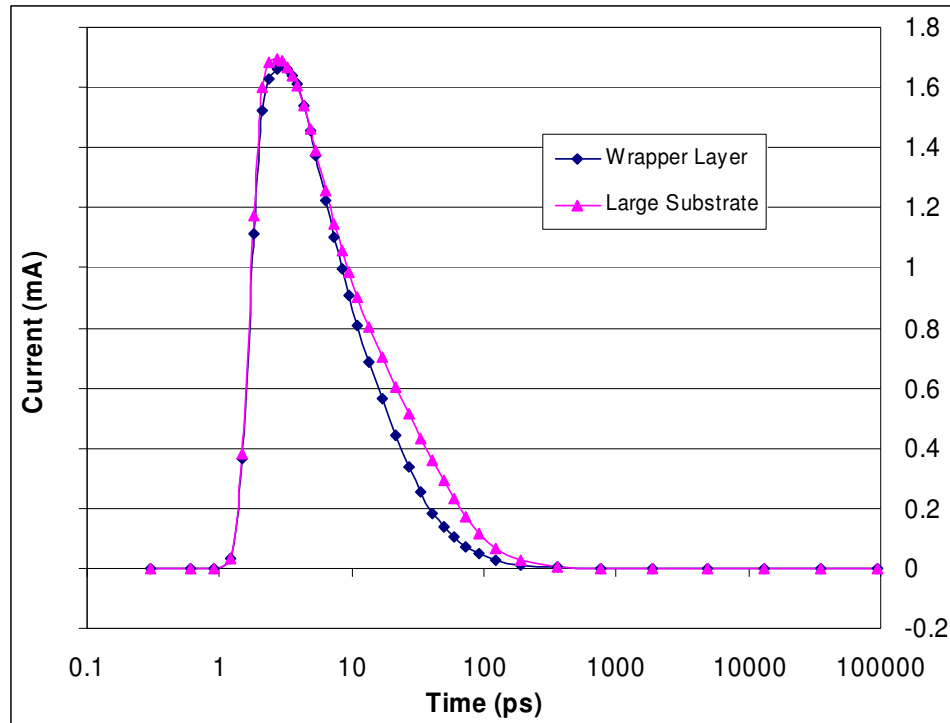


Figure 32: nFET Drain current from Drain Hit with Carbon ion ($LET=3.4 \text{ MeV-cm}^2/\text{mg}$)

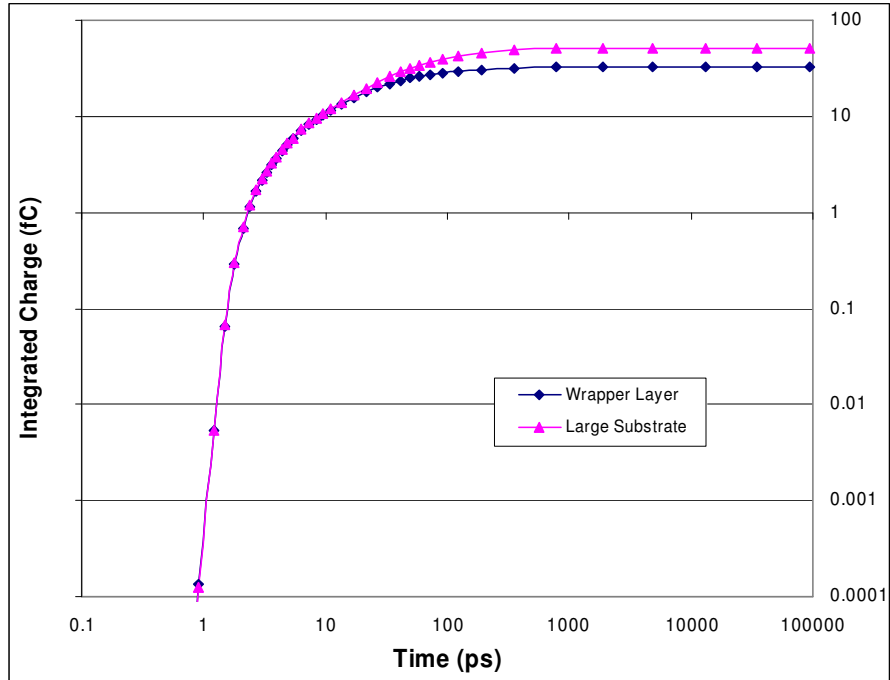


Figure 33: nFET Charge collection from Drain hit of Carbon ion (LET 3.4 MeV-cm²/mg)

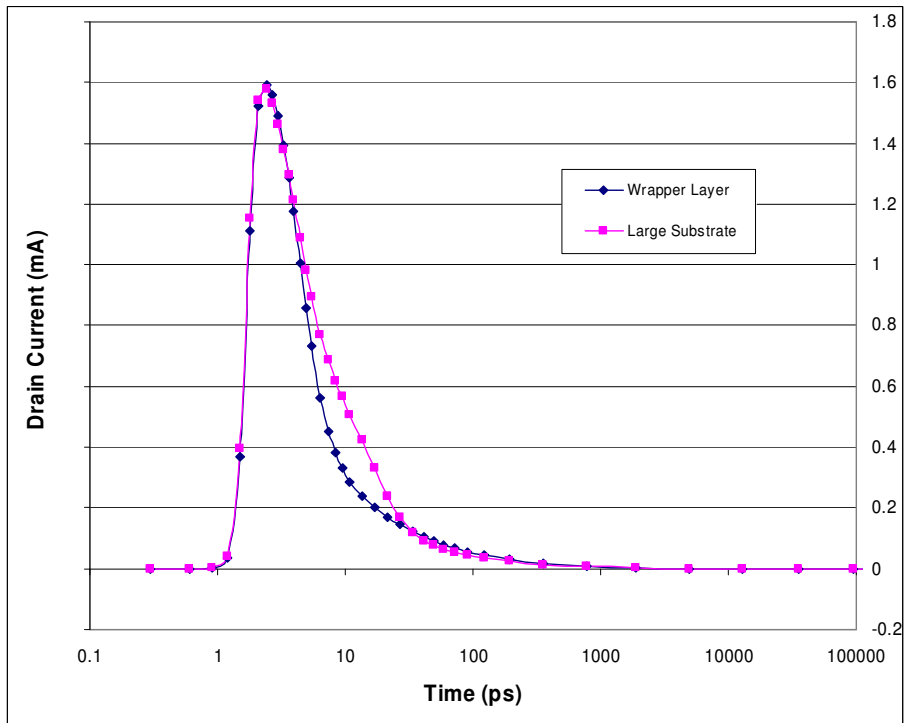


Figure 34: pFET Drain current from Drain Hit with Carbon ion (LET=3.389 MeV-cm²/mg)

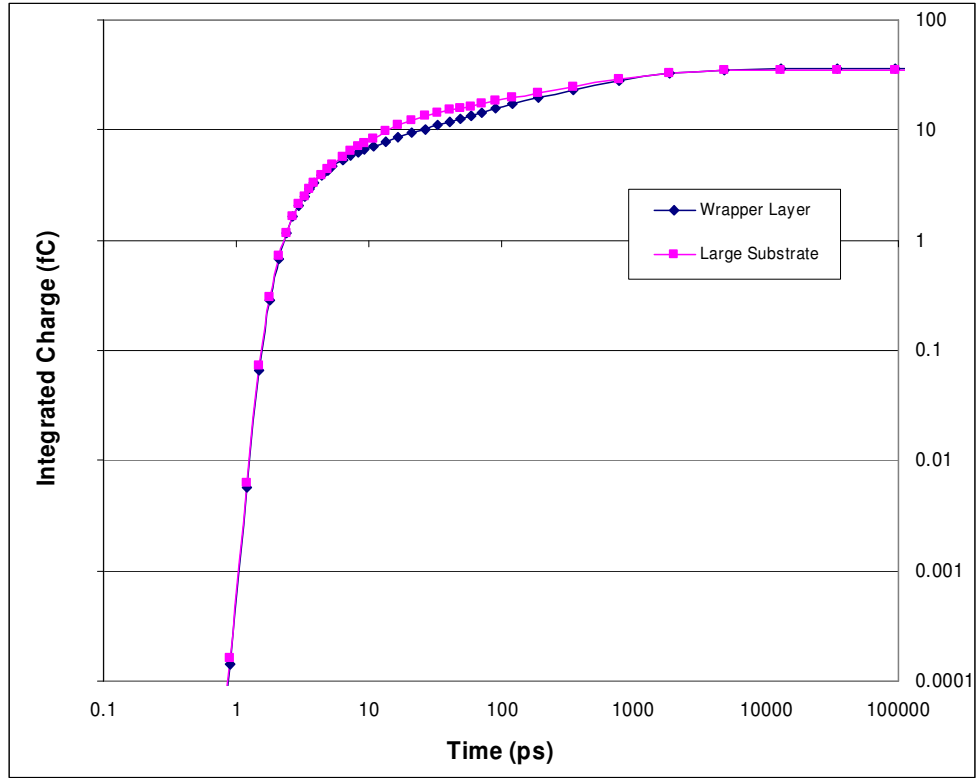


Figure 35: nFET Charge collection from Drain hit of Carbon ion (LET 3.389 MeV-cm²/mg)

As can be seen in the figures, both geometries, for the nFET and pFET, display a relatively similar amount of charge collection. Therefore the 3D geometry of the TCAD nFET and pFET implementing the wrapper layer was used for the charge collection data comparison.

Simulation Setup

Ion strike simulations were performed on the TCAD nFET and pFET chosen in the previous section. All the electrical characteristics from the devices calibrated for the I-V characteristic curves for the TCAD nFET and pFET were used in the SEE

simulations in order to compare them with the charge collection data. The only aspect that changed in the device was the meshing of the physical geometry. A slightly different meshing scheme was used when simulating the charge collection calibration. Figs. 36 and 37 show the meshing tight around the channel and around the areas of ion strike for the TCAD nFET. This allowed for a better convergence of the simulations involving Single Events.

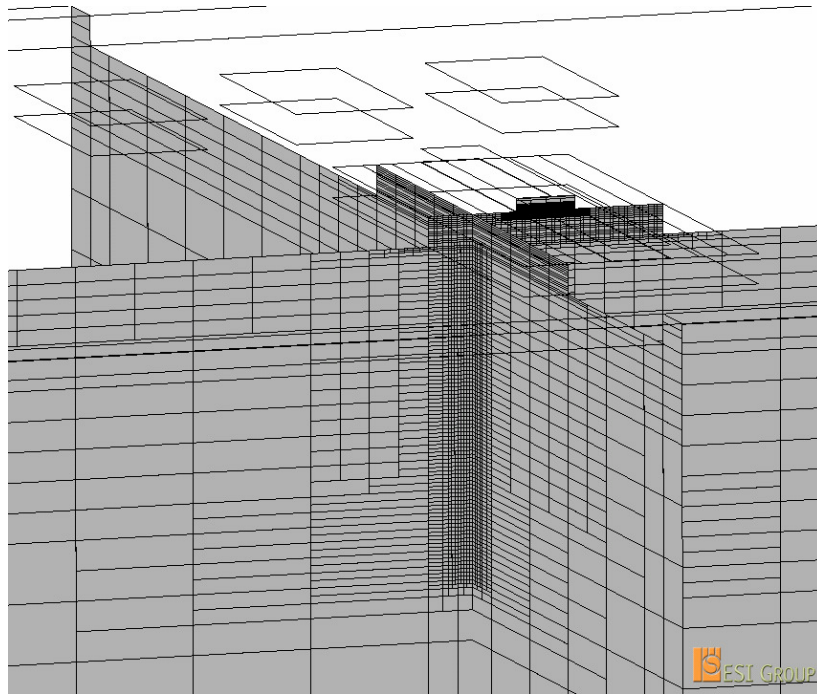


Figure 36: Cross sections in the X and Y directions showing the mesh refinements for an ion strike on the Drain of an nFET

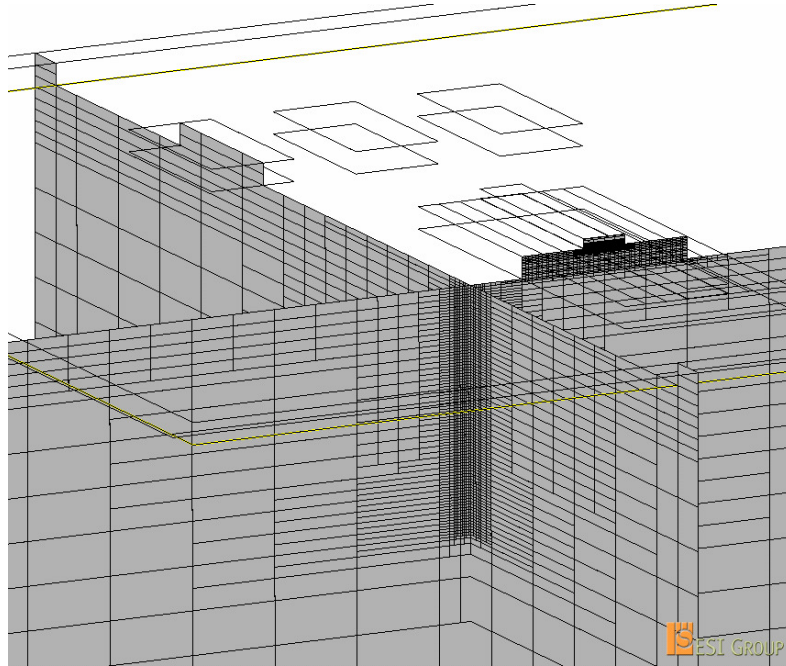


Figure 37: Cross sections in the X and Y directions showing the mesh refinements for an ion strike 2 μm outside of the Drain of an nFET

The refinement commands for these meshing refinements can be found in the Appendix. The locations chosen for the ion strikes were used to compare the charge collection with the data obtained experimentally. Since the beam scanned areas across the device in the experiment, in order to simplify the simulation setup, ion hits were placed in multiple locations of the TCAD nFET and pFET and compared to the measured data.

The ion strikes for the charge collection simulations were given the radiation characteristics shown in Table 1.

		NMOS		PMOS	
DC Bias Conditions		$V_d = 3V, V_g = 0V$ $V_s = 0V, V_b = 0V$		$V_d = -3V, V_g = 0V$ $V_s = 0V, V_b = 0V$	
Hit Location		Drain	Drain + 2um	Drain	Drain + 2um
Strike Coordinates (microns)	X	-1.25	-3.25	0.75	-1.25
	Y	-5	-5	-5	-5
	Z	10	10	11.5	11.5
Gaussian Decay Radius (microns)		0.1	0.1	0.1	0.1
Ion Track Depth (microns)		2 and 5	2 and 5	2 and 5	2 and 5
Ion Strike Peak Time (ps)		1.5	1.5	1.5	1.5
Ion Strike Sigma (ps)		0.25	0.25	0.25	0.25
Ion Strike LET (MeV-cm²/mg)	Carbon Oxygen	3.389 6.199	3.389 6.199	3.389 6.199	3.389 6.199

Table 1: Details of Radiation Ion Strike simulations

The LET values for carbon and oxygen shown in the table above were determined from a program called The Stopping and Range of Ions in Materials (SRIM)²⁹. The SRIM program calculated an LET of 2.944 MeV-cm²/mg for a Carbon ion with energy of 36 MeV and an LET of 5.378 MeV-cm²/mg for an Oxygen ion with energy of 36 MeV. However, as shown in Fig. 38, after taking into account 10 μ ms of interconnections from the top of packaged device to the nFET and pFET, the resulting higher LET values, shown in Table 1, were determined for Carbon and Oxygen.

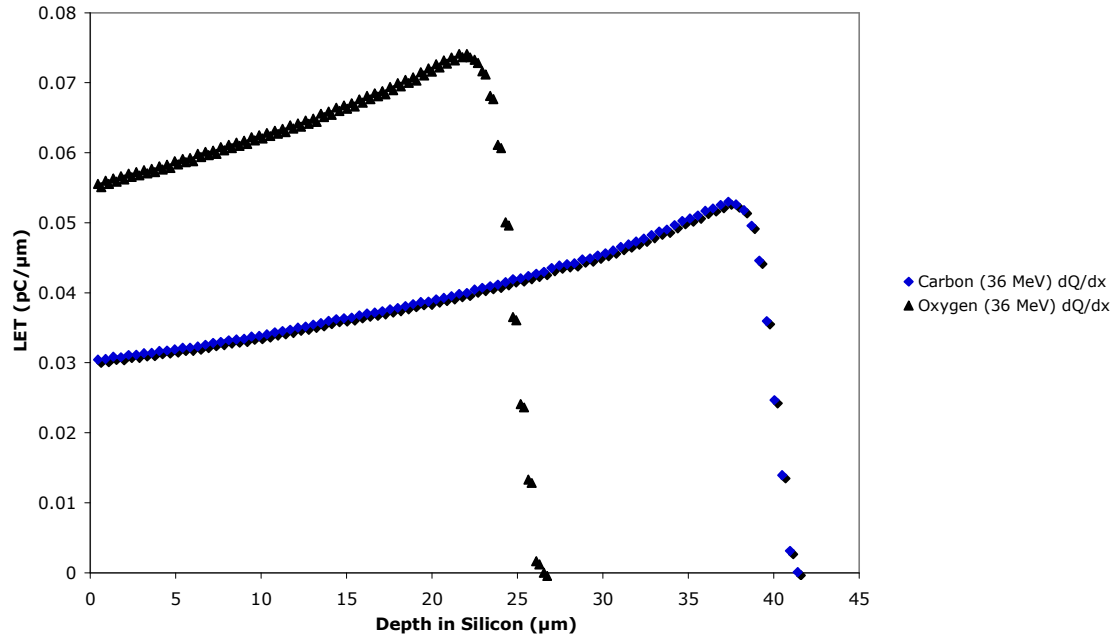


Figure 38: SRIM Calculations of Carbon and Oxygen²⁹

For the simulation, the ion strike locations were chosen to focus the hits directly in the center of the Drain and 2 microns outside of the Drain. The CFD-ACE-GUI models the ion track as a cylindrical column of excess charge which can be specified as either a uniform or Gaussian radial profile³⁰. A Gaussian profile was chosen because of the increased accuracy that has been found with it compared to the uniform profile³¹. The value of 100 nm was chosen for the decay radius because of the accuracy found in this type of Gaussian profile. Since the well depth was approximately 1 – 1.5 μms deep, the ion track depths of 2 μm and 5 μm were chosen to see if there was a significant difference in charge collection between these two depths. The ion strike peak time refers to the time at which the charge deposited by the ion strike is at the highest. A time of 1.5 ps was used to allow for enough time to have the charge build up before the peak as

indicated by the ion strike sigma. This variable controls the 1/e decay of the Gaussian function in time³⁰.

Results

The solver, NanoTCAD, performed transient simulations of the ion strikes on the TCAD nFET and pFET, with the ion strike characteristics shown above in Table 1. The resulting charge collection of the TCAD nFET and pFET can be seen as Table 2 alongside the charge collection data²⁸.

		nFET Charge Collection data (pC)		pFET Charge Collection Data (pC)	
		<i>Measured</i>	<i>Simulated</i>	<i>Measured</i>	<i>Simulated</i>
Oxygen	<i>Drain</i>	0.1 - 0.075	0.095	0.2 - 0.14	0.175
	<i>Drain + 2um</i>	0.45 – 0.02	0.025	0.035 – 0.005	0.015
Carbon	<i>Drain</i>	0.07 – 0.04	0.055	0.115 -0.095	0.11
	<i>Drain + 2um</i>	0.145 – 0.09	0.089	0.085 – 0.05	0.055

Table 2: Comparison of measured charge collection data vs. simulated charge collection data

As can be seen on the table above the charge collection of the TCAD devices match well when compared to the experimental data as well as the similarity of the spatial charge collection. The most charge for the devices was collected on or extremely near the Drain of either device. The farther away the ion strikes from the Drain, the less charge either device collected. When comparing the hits at different depths for the

simulations, it was observed that the charge collected by either depth were within 10% of each other. These results have shown that the TCAD nFET and pFET match the physical 5AM nFET and pFET.

CHAPTER V

MIXED-MODE COMPARISONS OF AN SRAM CELL AT COLD TEMPERATURES

Introduction

In order to see simulate the SE response of the SRAM cell at cold temperatures, the TCAD nFET and pFET, designed in the previous chapter, were implemented in an SRAM cell containing the same characteristics, albeit different physical dimensions. The SRAM cell design and layout came from the University of Arkansas. The cold temperature spice parameters, developed by Lynguent Technologies, were calibrated models based on experimental data obtained from physical devices operating in cold temperatures. A schematic representation of the SRAM is shown as Fig. 39 as well as the layout of the SRAM shown as Fig. 40. The design of the SRAM was implemented with the design rules from the IBM SiGe 5AM BiCMOS process technology. As explained in Chapter II, the effect being measured from the cold temperature variable is to see whether the critical charge decreases at lower temperatures causing the SRAM to flip. This chapter will show the critical charge of the SRAM implementing both the TCAD nFET and pFET will decrease as the temperature is decreased.

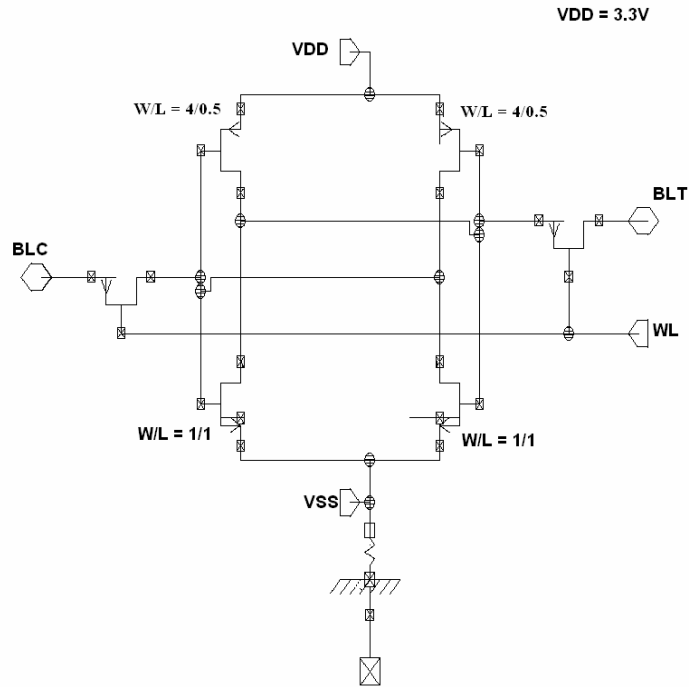


Figure 39: Schematic of the SRAM cell developed by the University of Arkansas implementing the IBM 5AM process

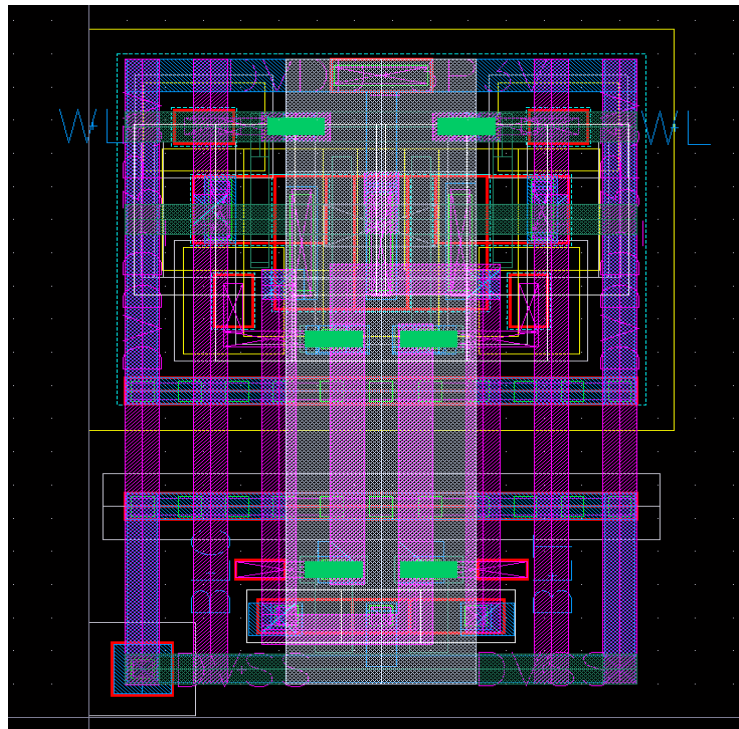


Figure 40: Layout of the SRAM developed by the University of Arkansas implementing the IBM 5AM process

Determining Upset LET

Simulation Setup

For this phase of the simulation process, the MixCAD program, described in Chapter III, was used in order to perform the necessary mixed-mode simulations. These simulations required a Spectre netlist, which implements the Spectre circuit information, to be executed within the .cir (circuit) files. Within these files, the spice circuit parameters, pin connections, and transient simulation variables are contained. The circuit files used to perform these simulations as well as the spice parameters for the IBM 5AM CMOS devices can be found in the Appendix. A visual representation of the circuit simulations implementing both the TCAD nFET and pFET can be seen as Figs. 41 and 42. The circuits were set up this way in order to capture the most sensitive regions in TCAD for both circuits implementing the nFET and pFET.

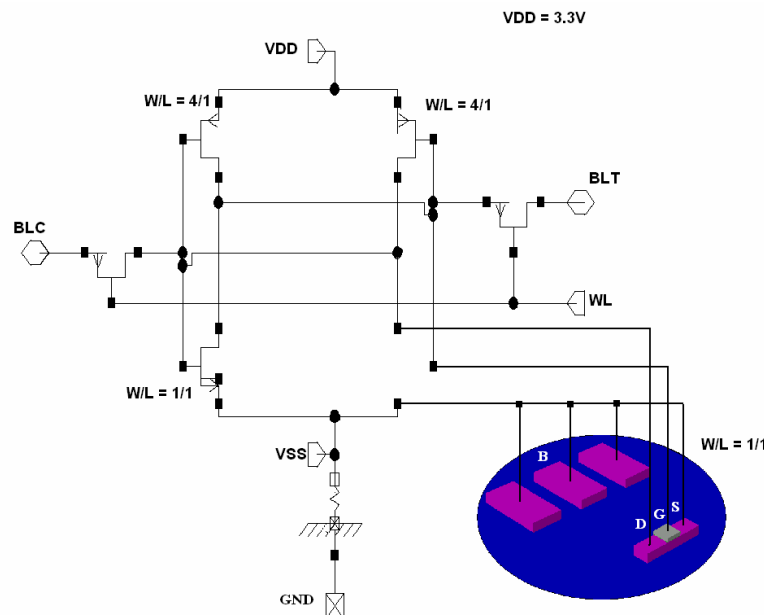


Figure 41: Schematic representation of the Spice devices implemented with the 3D nFET TCAD device.

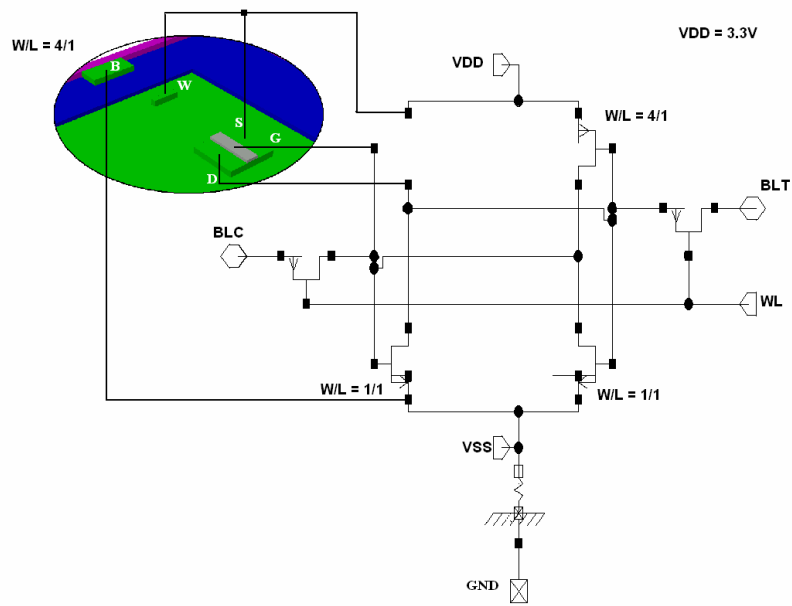


Figure 42: Schematic representation of the Spice devices implemented with the 3D pFET TCAD device

The process of obtaining the upset LET required several rounds of mixed-mode simulations. The ion strike was located directly on the drain to a depth of 2 μm . This value was chosen because, as indicated from the simulated charge collection data, there was no significant difference in charge collection between the depths of 2 and 5 μm s. The LET values were chosen arbitrarily in order to obtain the upper and lower bounds of

the LET that would cause the SRAM to upset. After the first round of simulations, it was determined that the upset LET was between 7 and 17 MeV-cm²/mg for the nFET and between 20 and 33 MeV-cm²/mg for the pFET. Multiple iterations were used to determine that an LET of 15 MeV-cm²/mg for the nFET and 25 MeV-cm²/mg for the pFET caused the SRAM to upset at 300K.

The resulting voltage input, voltage outputs, and integrated charge for the two SRAM circuits indicating an the LET value which deposited enough charge to flip the SRAM operating at nominal temperature can be seen as in the Results section below.

Results for SRAM cell implementing 3D TCAD nFET at Nominal Temperature

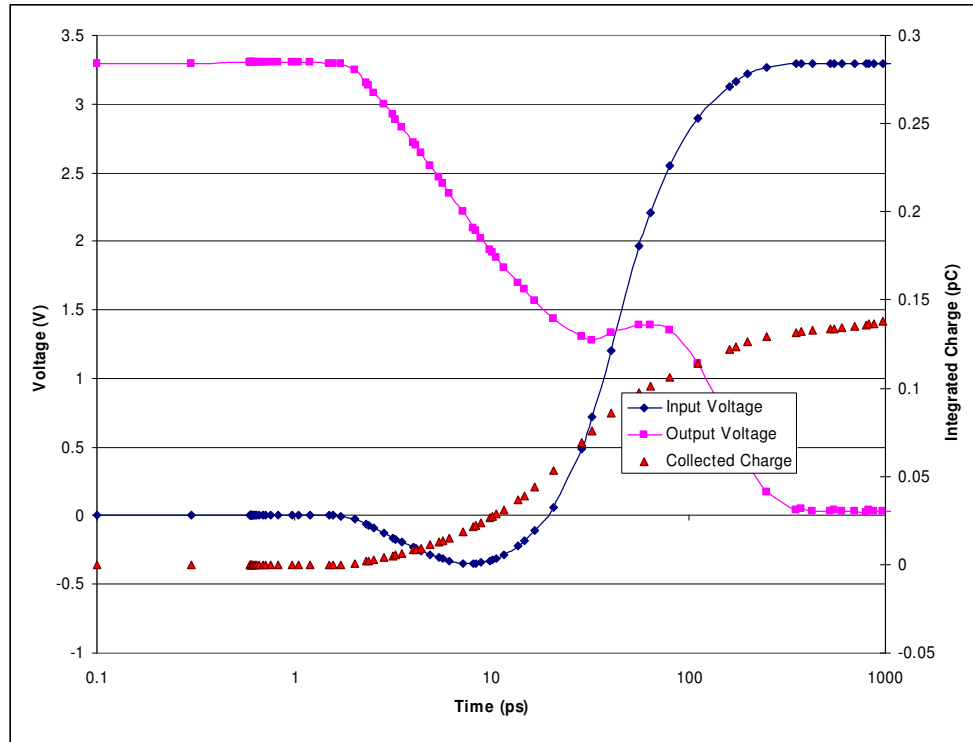


Figure 43: Graph of the input voltage, output voltage, and integrated charge of the SRAM implementing the 3D TCAD nFET with the following characteristics: $V_d=3.3V$, $V_g=0V$ – ion strike, peak at 2.0 ps, LET = 15 MeV-cm²/mg

From this graph, it can be seen that an ion with LET = 15 MeV-cm²/mg striking the SRAM cell implementing a 3D TCAD nFET deposited enough charge to cause an SEU in the SRAM at 300K. The integrated charge is also shown in Fig. 43. This graph was obtained by integrating the drain current of the TCAD device. On that graph, the point in time in which enough charge was collected by the SRAM to cause the input and output to flip was the critical charge³². In this simulation at 300K the critical charge was 0.103 pC. The upset LET of 15 MeV-cm²/mg is a sufficient parameter as it characterizes the type of ion required to cause an upset in the SRAM cell.

Results for SRAM cell implementing 3D TCAD pFET at Nominal Temperature

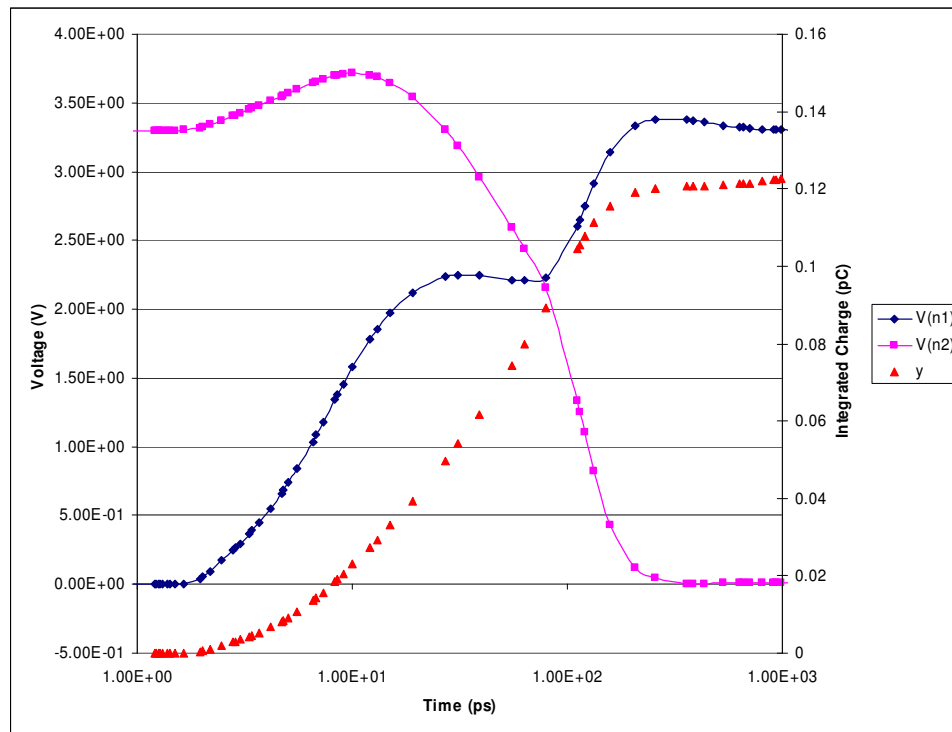


Figure 44: Graph of the input voltage, output voltage, and integrated charge of the SRAM implementing the 3D TCAD pFET with the following characteristics: $V_d = -3.3V$, $V_g = 0V$ – ion strike, peak at 2.0 ps, LET = 25 MeV-cm²/mg

From this graph, it can be seen that an ion with $LET = 25 \text{ MeV-cm}^2/\text{mg}$ striking the SRAM cell implementing a 3D TCAD pFET deposited enough charge to cause an SEU in the SRAM at 300K. In this graph, the integrated charge curve was plotted by integrating the drain current of the TCAD device. The point in time in which enough was collected to cause the input and output to flip was called the critical charge³². For this SRAM circuit, the critical charge was 0.12 pC. As mentioned for the nFET, the input LET is a useful measurement as it indicates the type of ion required to cause a strike on the pFET causing an upset in the SRAM cell.

Cold Temperature Simulations at Upset LET

Simulation Setup

The next set of simulations was conducted in order to determine if the critical charge for SEU's in the SRAM cells decreased as the temperature is decreased. The software provided by CFD and ESI have the ability to perform TCAD simulations with a wide range of temperatures. The graph below shows the types of models, and the references to researched data, that were implemented into the TCAD solvers in order to model the cold temperature effects³³.

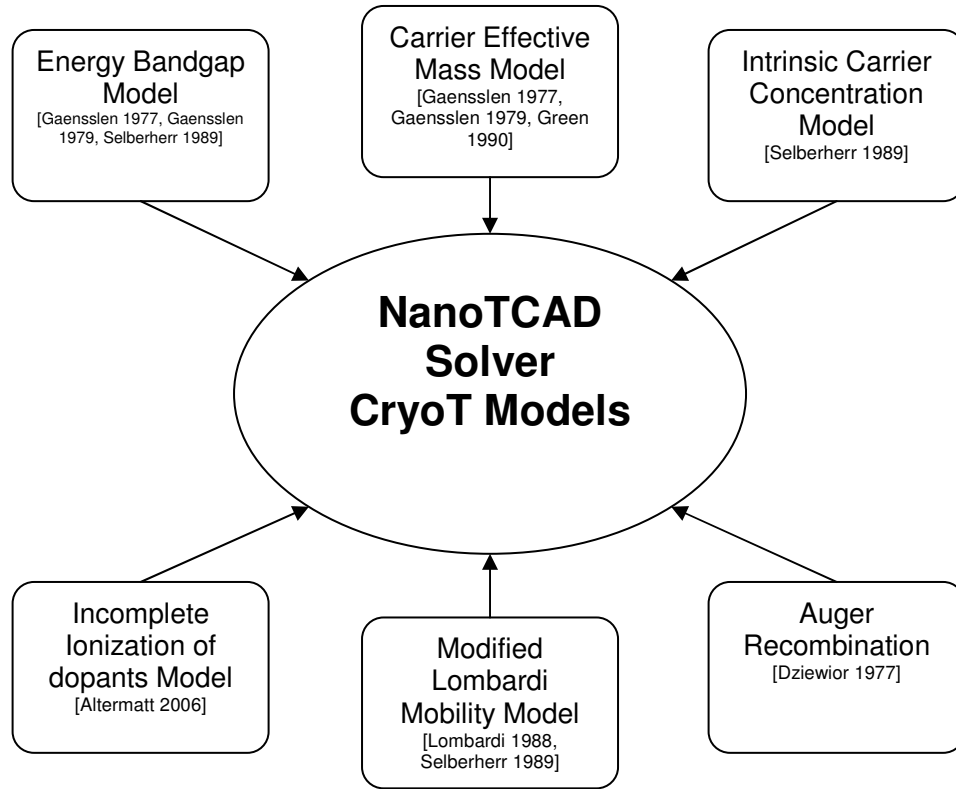


Figure 44: Indicates the cold temperature models used in the CFDRC NanoTCAD solvers³³

Additionally, the spice parameters of the IBM SiGe 5AM nFET and pFET operating at cold temperatures were also available for use in these simulations. The spice parameters for the Spectre software were changed in order to reflect the attributes of cold temperature afflicting the IBM SiGe 5AM BiCMOS process technology. These parameters were provided by Lynguent Technologies. The spice parameter files with the incorporated cold temperatures can be found at in the Appendix.

The first step in this process was to change the temperature variables in both software programs to reflect the cold temperature at that step. The SRAM cell was simulated with cold temperatures of 275K (2°C), 250K (-23°C), 237K (-23°C), 225K (-

48°C), 212K (-61°C), 200K (-73°C), 187K (-86°C), 175K (-98°C), 150K (-123°C) and 100K (-173°C).

The next step was to determine the LET which deposited enough charge flip the SRAM as was done with the simulation performed at 300K. From there the critical charge for the SRAM cells can be determined. The method to determine these values was achieved through the same process as the simulation set at 300K described in the previous section.

Results

The plots below, shown as Figs. 46 and 47, shows the critical charge and upset LET for the SRAM, implementing both an nFET and pFET, simulated at the cold temperature ranges for which spice parameters were available.

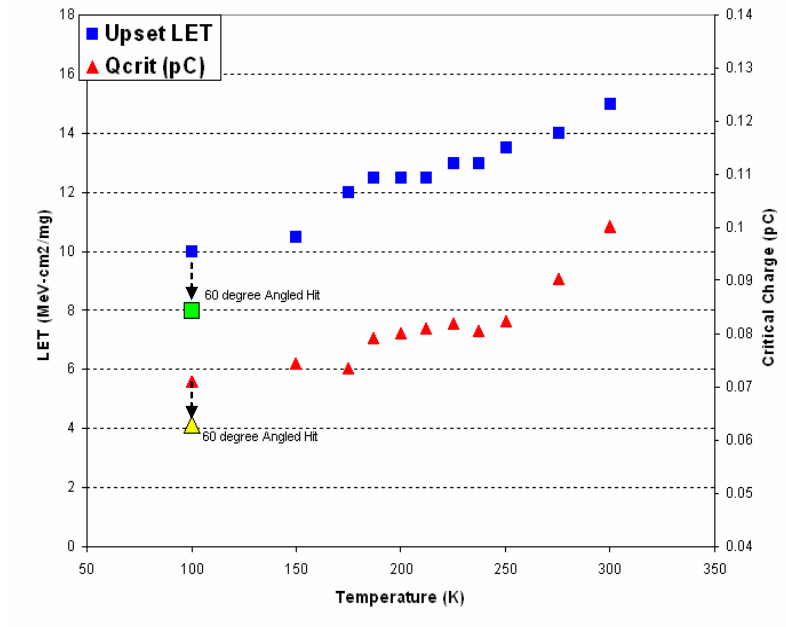


Figure 45: Critical Charge vs. Temperature. This shows how both the critical charge and upset LET decreases as the temperature decreases for the SRAM cell implementing the nFET

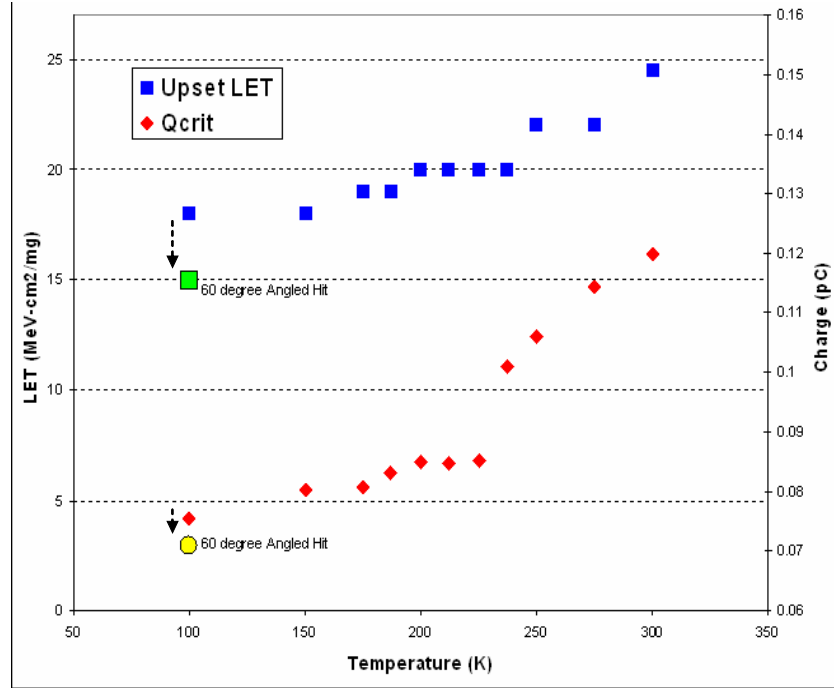


Figure 46: Critical Charge vs. Temperature. This shows how both the critical charge and upset LET decreases as the temperature decreases for the SRAM cell implementing the pFET

Also displayed on the plots above is the “worse” case scenario with an ion strike simulated with a 60° angled hit on the drain at 100K. It can be seen that the upset LET and the critical charge for both the nFET and pFET decrease compared to the strike at normal incidence.

The plots shown below display the change in peak current as a function of temperature. Fig. 47 shows the output current at the drain of the TCAD device at 100K and 300K. Fig. 48 shows the peak current increasing as the temperature is decreased.

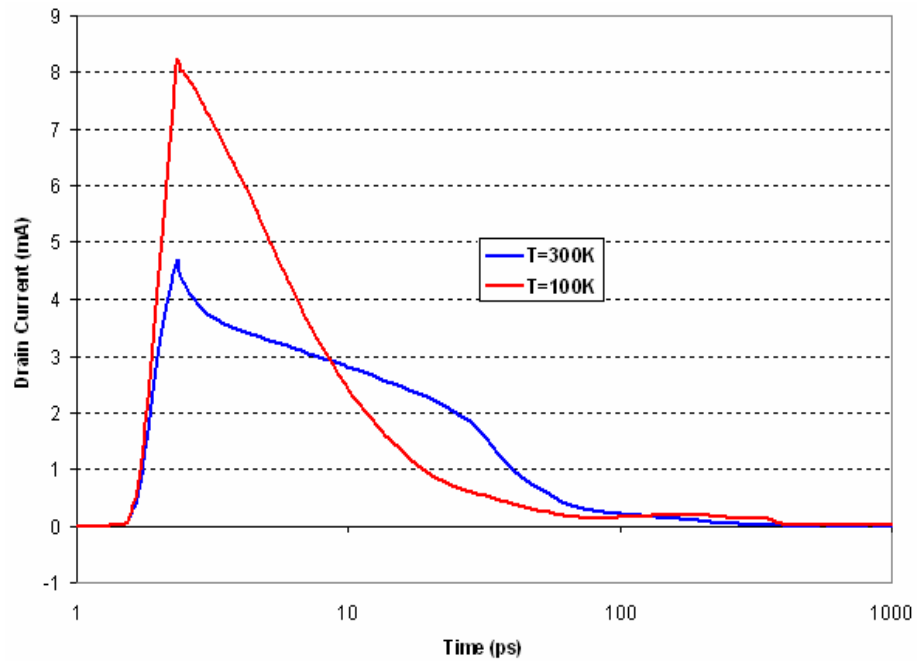


Figure 47: Output of drain current at struck node for 300K and 100K

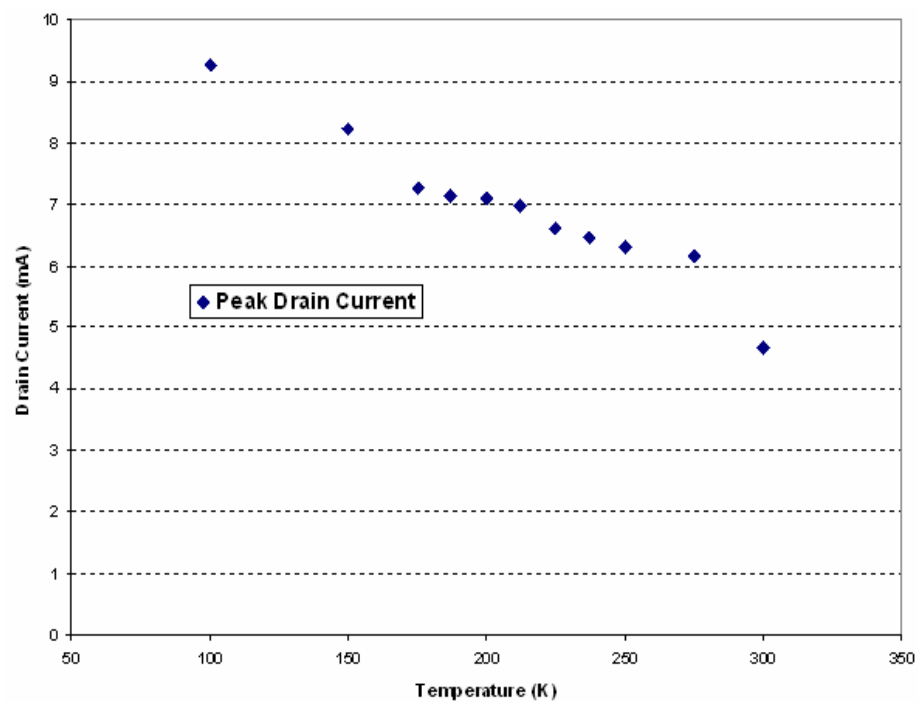


Figure 48: Relationship of peak current and temperature.

Discussion

The trend in the graphs above indicates an overall drop in critical charge for decreased temperatures. This represents an approximate 30% decrease in charge needed to cause the SRAM to flip for the nFET and an approximate 35% decrease in charge for the pFET for the same affect. This could cause reliability issues for SRAM cells chosen for operation in extreme environments even with a certain amount of radiation hardening. Additionally, Figs. 47 and 48 show an increase in peak currents at lower temperatures. Since the upsets are occurring quickly (in picoseconds), even at 300K. The drift current component plays a significant role in the upset mechanism for the SRAM. The increased peak currents shown at lower temperatures can make these peak currents play an even more important role as the temperature is decreased.

Although the upset LET for both the nFET and pFET decrease as the temperature is decreased, the drop in upset LET is still above sub-critical LET values that were of concern for this SRAM. If the error management systems implemented in the SRAM cell were developed to withstand low LET particles, i.e. protons, and therefore no additional radiation hardening will be needed for the SRAM as the temperature is decreased below values common to commercial and even mil-spec electronics.

CHAPTER IV

CONCLUSIONS

This research has shown through mixed-mode simulation, the critical charge for an SRAM cell designed in the SiGe BiCMOS process decreases at cold temperatures. In some cases the decrease can be as great as 30% of critical charge simulated at 300K. Also, there is an increased influence of the drift current component due to the higher mobilities as the temperature is decreased.

The modeling of cold temperature effects and calibration of the IBM 5AM SiGe BiCMOS process technology were essential in this research. The TCAD solvers were chosen because of their seamless compatibility between the spice models used in this research. Furthermore, the built-in models of the TCAD solvers and the compact models of the spice parameters, both calibrated based on experimental physical devices at cold temperatures, provided additional tools in studying the SRAM cell at cold temperatures.

These tools were a useful way of building and calibrating the TCAD devices to the IBM 5AM devices. Furthermore, the cold temperature models for the TCAD solver and spice circuit simulator proved to be an effective means of predicting the SEU sensitivity of the SRAM at lower temperatures. By simulating temperature effects with the calibrated spice and TCAD models for the SRAM cell, it can be concluded the level of charge needed to cause an upset in the circuit decreases as the temperature is decreased.

This brings attention to whether the error management system is sufficient at cold temperatures for the memory block. According to the design from the University of

Arkansas, the SRAM should be tolerant of low LET events ranging in the single digits MeV-cm²/mg. Therefore, no additional radiation hardening on the cell level for the memory unit would be necessary in guarding against the sub-critical LETs, i.e. protons, even at low temperatures and therefore the error management system is sufficient. Furthermore, these simulations should provide the needed guidance for the future experiments intended to obtain empirical data on the SRAM cell.

APPENDIX

Micromesh – Mesh Refinement Files

The following files contain coordinates of section in their respective files in voxels to refine that area to a specific voxel amount. The first three numbers represent the bottom, nearest, left voxel (X-Y-Z) of that section; the second three numbers represent the top, farthest, right voxel (X-Y-Z) of that section; the next three numbers represent the amount of refinement in voxels (X-Y-Z) wanted in the area sectioned with the first two sets of numbers; the final three numbers represent the enlargement factor which increase in voxels (X-Y-Z) that section to match the section it borders.

Mesh Refinement of 3D TCAD 10 um x 1um nFET

```
MeshSize3txt v1.0
0 0 2125 640 640 2500 20 40 75 2 2 2
280 120 2375 360 320 2500 2 20 15 10 1 5
310 120 2475 330 320 2520 1 20 3 2 1 5
```

Mesh Refinement of 3D TCAD 10 um x 1um pFET

```
MeshSize3txt v1.0
0 0 2500 1040 1040 2875 20 40 75 2 2 2
370 305 1125 670 735 2875 20 20 150 1 2 2
520 345 2750 600 545 2875 2 20 15 2 1 10
540 345 2850 580 545 2895 1 20 3 2 1 5
```

Mesh Refinement of 3D TCAD 10 um x 1um nFET for drain hit

```
MeshSize3txt v1.0
0 0 2125 640 640 2500 20 40 75 2 2 2
200 280 1500 400 360 2500 20 20 75 1 2 1
260 120 1500 340 320 2500 10 20 75 2 1 1
```

```

280 120 2375 360 320 2500 2 20 15 10 1 5
310 120 2475 330 320 2520 1 20 3 2 1 5
290 215 1000 300 225 2375 1 4 25 1 5 3

```

Mesh Refinement of 3D TCAD 10 um x 1um nFET for drain + 2um hit

MeshSize3txt v1.0

```

0 0 2125 640 640 2500 20 40 75 2 2 2
160 280 1500 360 360 2500 20 20 75 1 2 1
220 120 1500 300 320 2500 10 20 75 2 1 1
280 120 2375 360 320 2500 2 20 15 10 1 5
310 120 2475 330 320 2520 1 20 3 2 1 5
250 215 1000 260 225 2375 1 4 25 1 5 3

```

Mesh Refinement of 3D TCAD 10 um x 1um pFET for drain hit

MeshSize3txt v1.0

```

0 0 2500 1040 1040 2875 20 40 75 2 2 2
370 305 1125 670 735 2875 20 20 150 1 2 2
440 305 1125 640 585 2875 20 20 75 1 1 2
500 345 1125 580 545 2875 10 20 75 2 1 1
520 345 2750 600 545 2875 2 20 15 2 1 10
540 345 2850 580 545 2895 1 20 3 2 1 5
530 440 1375 540 450 2750 5 10 6 4 2 2

```

Mesh Refinement of 3D TCAD 10 um x 1um pFET for drain + 2um hit

MeshSize3txt v1.0

```

0 0 2500 640 640 2875 20 40 75 2 2 2
265 100 1125 415 415 2875 20 20 75 1 2 2
260 100 1125 360 340 2875 20 20 75 1 1 2
290 120 1125 330 320 2875 10 20 75 2 1 1
340 120 2750 380 320 2874 2 20 15 2 1 10
350 120 2850 370 320 2895 1 20 3 2 1 5
290 215 1375 300 225 2750 1 4 75 4 2 2

```

Mesh Refinement of 3D TCAD 10 um x 1 um nFET with large substrate

MeshSize3txt vl.0

```
0 0 7375 1280 1280 7750 20 40 75 2 2 2
520 600 6750 720 680 7750 20 20 75 1 2 1
580 440 6750 660 640 7750 10 20 75 2 1 1
600 440 7625 680 640 7750 2 20 15 10 1 5
630 440 7725 650 640 7770 1 20 3 2 1 5
610 535 6750 620 545 7625 1 4 25 1 5 3
```

Mesh Refinement of 3D TCAD 10 um x 1 um pFET with large substrate

MeshSize3txt vl.0

```
0 0 7375 1280 1280 7750 20 40 75 2 2 2
490 400 6250 790 830 7750 20 20 75 1 2 2
560 400 6250 760 680 7750 20 20 75 1 1 2
620 440 6250 700 640 7750 10 20 75 2 1 1
640 440 7655 720 640 7750 2 20 15 2 1 10
660 440 7725 700 640 7770 1 20 3 2 1 5
650 535 6250 660 545 7625 1 4 75 4 2 2
```

Mesh Refinement of 3D TCAD 1 um x 1 um nFET used with SRAM cell

MeshSize3txt vl.0

```
0 0 2125 640 640 2500 20 40 75 2 2 2
280 280 1500 400 360 2500 20 20 75 1 2 1
340 300 1500 340 320 2500 10 10 75 2 2 1
280 300 2375 360 320 2500 2 10 15 10 1 5
310 300 2475 330 320 2520 1 10 3 2 1 5
290 305 1500 300 315 2375 1 4 25 1 5 3
```

Mesh Refinement of 3D TCAD 4 um x 0.5 um pFET used with SRAM cell

MeshSize3txt vl.0

```
0 0 2500 640 640 2875 20 40 75 2 2 2
265 150 1125 415 415 2875 20 20 75 1 2 2
270 150 1125 400 340 2875 20 20 75 1 1 2
```

```

300 170 1125  370 320 2875  10 20 75  2 1 1
320 240 2750  390 320 2874  2 20 15  2 1 10
350 240 2850  360 320 2895  1 20 3   2 1 5
330 275 1750  340 285 2750  1 4 75   4 2 2

```

CFD-ACE-GUI – Doping Profile Files

Doping profiles are added to the physical structure after the aspects of the simulation is entered in CFD-ACE-GUI. The units for each of the variables are outlined in each of the .doping files.

Doping Profile of 3D TCAD 10 um x 1 um nFET used for I-V calibration and charge collection measurements

```

Doping *** Dimensions in meters, Concentrations in 1/cm3 ***
Number of Wells
13
Well # 1 ===== (Substrate)
Method
1
Hole Concentration
-1E15
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-16E-6 16E-6 -16E-6 16E-6 1E-18 10.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 2 ===== (Substrate EPI)
Method
1
Hole Concentration
-1E16
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-15E-6 15E-6 -15E-6 15E-6 8.5E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 3 ===== (P Well)
Method
1
Hole Concentration
-5E16
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-4.5E-6 4.5E-6 -10E-6 10E-6 8.5E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 4 ===== (PolySilicon Gate)
Method
1
Electron Concentration
1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-0.5E-6 0.5E-6 -10E-6 0 10.01E-6 10.225E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-10

```

```

Well # 5 ===== (Retrograde Epi Profile)
Method
1
Hole Concentration
-1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-15E-6 15E-6 -15E-6 15E-6 9E-6 9E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.174E-6
Well # 6 ===== (P Well Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-4.5E-6 -2.5E-6 5E-6 9E-6 9.8E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.011E-6
Well # 7 ===== (P Well Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-1E-6 1E-6 5E-6 9E-6 9.8E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.011E-6
Well # 8 ===== (P Well Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
2.5E-6 4.5E-6 5E-6 9E-6 9.8E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.011E-6
Well # 9 ===== (Drain)
Method
1
Electron Concentration
1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-2E-6 -0.6E-6 -10E-6 0 9.7E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43.4E-9 1E-10
Well # 10 ===== (Source)
Method
1
Electron Concentration
1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
0.6E-6 2E-6 -10E-6 0 9.7E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43.4E-9 1E-10
Well # 11 ===== (Drain LDD)
Method
1
Electron Concentration
1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-0.725E-6 -0.475E-6 -10E-6 0 9.85E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28.3E-9 1E-10

```

```

Well # 12 ===== (Source LDD)
Method
1
Electron Concentration
1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
0.475E-6 0.725E-6 -10E-6 0 9.85E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28.3E-9 1E-10
Well # 13 ===== (Vt Implant)
Method
1
Hole Concentration
-1.8E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-0.15E-6 0.15E-6 -10E-6 0 9.925E-6 9.96E-6
Decay Distances(Dx,Dy,Dz)
1E-10 1E-10 1E-10

```

Doping Profile of 3D TCAD 10 um x 1 um pFET used for I-V calibration and charge collection measurements

```

Doping *** Dimensions in meters, Concentrations in 1/cm3 ***
Number of Wells
11
Well # 1 ===== (Substrate)
Method
1
Hole Concentration
-1E15
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-25E-6 25E-6 -25E-6 25E-6 1E-6 11E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 2 ===== (N Well)
Method
1
Electron Concentration
1E17
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-7.5E-6 7.5E-6 -10.75E-6 10.75E-6 9.5E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 3 ===== (Poly)
Method
1
Hole Concentration
-1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1.5E-6 2.5E-6 -8.75E-6 1.25E-6 11.51E-6 11.735E-6
Decay Distances(Dx,Dy,Dz)
1E-18 1E-18 1E-18
Well # 4 ===== (Substrate Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)

```

```

1E-18 4E-6 23E-6 25E-6 10.999E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 5 ===== (N Well Contact)
Method
1
Electron Concentration
2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1.75E-6 4E-6 8.25E-6 8.75E-6 11.3E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
10E-9 10E-9 10E-9
Well # 6 ===== (N Well Analytical Profile)
Method
1
Electron Concentration
3.5E17
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-7.5E-6 7.5E-6 -10.75E-6 10.75E-6 10.5E-6 10.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.026E-6
Well # 7 ===== (Source)
Method
1
Hole Concentration
-1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
2.75E-6 4E-6 -8.75E-6 1.25E-6 11.2E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43E-9 1E-9
Well # 8 ===== (Drain)
Method
1
Hole Concentration
-1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1E-18 1.25E-6 -8.75E-6 1.25E-6 11.2E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43E-9 1E-9
Well # 9 ===== (Source LDD)
Method
1
Hole Concentration
-1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
2.425E-6 3E-6 -8.75E-6 1.25E-6 11.35E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28E-9 1E-9
Well # 10 ===== (Drain LDD)
Method
1
Hole Concentration
-1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1E-6 1.575E-6 -8.75E-6 1.25E-6 11.35E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28E-9 1E-9
Well # 11 ===== (Vt Implant)
Method
1
Electron Concentration
4.5E17
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)

```

```

1.95E-6 2.05E-6 -8.75E-6 1.25E-6 11.4E-6 11.45E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9

```

Doping Profile of 3D TCAD 1 um x 1 um nFET used in SRAM cell

```

Doping *** Dimensions in meters, Concentrations in 1/cm3 ***
Number of Wells
13
Well # 1 ===== (Substrate)
Method
1
Hole Concentration
-1E15
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-16E-6 16E-6 -16E-6 16E-6 1E-18 10.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 2 ===== (Substrate EPI)
Method
1
Hole Concentration
-1E16
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-16E-6 16E-6 -16E-6 16E-6 8.5E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 3 ===== (P Well)
Method
1
Hole Concentration
-5E16
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-4.5E-6 4.5E-6 -10E-6 10E-6 8.5E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 4 ===== (PolySilicon Gate)
Method
1
Electron Concentration
1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-0.5E-6 0.5E-6 -1E-6 1E-18 10.01E-6 10.225E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-10
Well # 5 ===== (Retrograde Epi Profile)
Method
1
Hole Concentration
-1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-15E-6 25E-6 -15E-6 15E-6 9E-6 9E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.174E-6
Well # 6 ===== (P Well Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-4.5E-6 -2.5E-6 5E-6 9E-6 9.8E-6 10E-6

```

```

Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.011E-6
Well # 7 ===== (P Well Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-1E-6 1E-6 5E-6 9E-6 9.8E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.011E-6
Well # 8 ===== (P Well Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
2.5E-6 4.5E-6 5E-6 9E-6 9.8E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.011E-6
Well # 9 ===== (Drain)
Method
1
Electron Concentration
1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-2E-6 -0.6E-6 -1E-6 1E-18 9.7E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43.4E-9 1E-10
Well # 10 ===== (Source)
Method
1
Electron Concentration
1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
0.6E-6 2E-6 -1E-6 1E-18 9.7E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43.4E-9 1E-10
Well # 11 ===== (Drain LDD)
Method
1
Electron Concentration
1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-0.725E-6 -0.475E-6 -1E-6 1E-18 9.85E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28.3E-9 1E-10
Well # 12 ===== (Source LDD)
Method
1
Electron Concentration
1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
0.475E-6 0.725E-6 -1E-6 1E-18 9.85E-6 10E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28.3E-9 1E-10
Well # 13 ===== (Vt Implant)
Method
1
Hole Concentration
-1.8E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-0.15E-6 0.15E-6 -1E-6 1E-18 9.925E-6 9.96E-6

```

```
Decay Distances(Dx,Dy,Dz)
1E-10 1E-10 1E-10
```

Doping Profile of 3D TCAD 4 um x 0.5 um pFET used in SRAM cell

```
Doping *** Dimensions in meters, Concentrations in 1/cm3 ***
Number of Wells
11
Well # 1 ===== (Substrate)
Method
1
Hole Concentration
-1E15
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-16E-6 16E-6 -16E-6 16E-6 1E-6 11E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 2 ===== (N Well)
Method
1
Electron Concentration
1E17
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-7.5E-6 7.5E-6 -12E-6 9.5E-6 9.5E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 3 ===== (Poly)
Method
1
Hole Concentration
-1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1.5E-6 2E-6 -4E-6 0 11.51E-6 11.735E-6
Decay Distances(Dx,Dy,Dz)
1E-18 1E-18 1E-18
Well # 4 ===== (Substrate Contact)
Method
1
Hole Concentration
-2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1E-18 4E-6 13E-6 15E-6 10.999E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9
Well # 5 ===== (N Well Contact)
Method
1
Electron Concentration
2E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1.75E-6 4E-6 7E-6 7.5E-6 11.3E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
10E-9 10E-9 10E-9
Well # 6 ===== (N Well Analytical Profile)
Method
1
Electron Concentration
3.5E17
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
-7.5E-6 7.5E-6 -12E-6 9.5E-6 10.5E-6 10.5E-6
```

```

Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 0.026E-6
Well # 7 ===== (Source)
Method
1
Hole Concentration
-1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
2.25E-6 3.5E-6 -4E-6 0 11.2E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43E-9 1E-9
Well # 8 ===== (Drain)
Method
1
Hole Concentration
-1E20
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1E-18 1.25E-6 -4E-6 0 11.2E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 43E-9 1E-9
Well # 9 ===== (Source LDD)
Method
1
Hole Concentration
-1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1.925E-6 2.5E-6 -4E-6 0 11.35E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28E-9 1E-9
Well # 10 ===== (Drain LDD)
Method
1
Hole Concentration
-1E18
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1E-6 1.575E-6 -4E-6 0 11.35E-6 11.5E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9 1E-9 28E-9 1E-9
Well # 11 ===== (Vt Implant)
Method
1
Electron Concentration
4.5E17
Sizes(x_left,x_right,y_low,y_high,z_top,z_bottom)
1.7E-6 1.8E-6 -4E-6 0 11.4E-6 11.45E-6
Decay Distances(Dx,Dy,Dz)
1E-9 1E-9 1E-9

```

MixCAD – Circuit Files

The circuit files are used to compile the spice parameters used in Spectre and couple them to the 3D TCAD outputs that come from NanoTCAD. Listed below are the details of the files that controlled the mixed-mode simulations of the SRAM cell

implementing both the nFET and pFET. Only the Test files are listed below, to recreate the files for the threshold LET simulations, the “PMOS_TEST.DTF” or “PMOS_TEST.DTF” command on Line 7 needs to be changed to the appropriate file name.

Circuit file of 3D TCAD nFET with the spice devices making up the SRAM cell

```
CFDRC Mixed-mode NanoTCAD simulation with ion strike

* 3D NanoTCAD simulation for struck 1-um NMOS device and
* SPICE models for the other 3 transistors in SRAM circuit.

* ACE NMOS 3D model for Spectre
.model nmos3D ACE model="NMOS_TEST.DTF"
+ pin1="electric:Sub_epi_DrainContact"
+ pin2="electric:PolySilicon_GateContact"
+ pin3="electric:Sub_epi_SourceContact"
+ pin4="electric:Sub_epi_SubstrateContact"
+ trace=3 pert=0.1V jacTolV=0.5V jacToli=1e-10 zero=1e-9 tol=2e-2
+ maxTimeStep=[0.3ps 3ps 0.5ps 5ps 1ps 10ps
+ 50ps 250ps 1e-10 1ns 1ns 1e-8 1e-6]
+ maxiter=20 skipFirst=1 maxvoltchg=0.125 currentMult=1

.options VABSTOL=10mV IABSTOL=10nA RELTOL=0.001

* SPICE NMOS and PMOS transistor models, with JUNCTION CAPACITANCES
.model nmos1 nmos (tnom=25 tox=0.0088E-6 xj=2.2E-7 nch=1.7E17 vth0=0.6
k1=0.76016 k2=-5.822152e-4
+ k3=5.0548281 k3b=5.0619266 w0=2.54204e-6 nlx=1.223643e-7 dvt0w=0
dvt1w=5.3e6 dvt2w=-0.032 dvt0=1.8396882
+ dvt1=0.6378645 dvt2=-0.44537 u0=435.0 ua=2e-13 ub=1.755743e-18
uc=9.12133e-11 vsat=1.006979e5
+ a0=1.0566486 ags=0.21 b0=1e-8 b1=9.89043e-8 keta=-4.239715e-3
a1=9.99316e-5 a2=1 rdsw=500
+ prwg=-4.096156e-4 prwb=0.0603814 wr=1 wint=0.12e-6 lint=0.055E-6
dwg=1.205029e-8 dwb=1.599025e-8
+ voff=-0.15 nfactor=1.3428907 cit=0 cdsc=-1e-3 cdsd=0 cdsb=-1e-4
eta0=0.2515419 etab=-0.02 dsub=1
+ pclm=0.5717291 pdiblc1=5.7744e-3 pdiblc2=3.422444e-3 pdiblc3=-0.1625042
drout=0.0851327 pscbe1=4.678648e8
+ pscbe2=5.097051e-4 pvag=0.025509 delta=0.01 alpha0=6.4E-6 beta0=24.5
js=1e-4 jsw=140E-12
+ ute=-1.35868 kt1=-0.3136 kt1l=7.3301e-9 kt2=-0.052227 ua1=3.01729e-9
ub1=-4.46905e-18 uc1=-5.6e-11 at=3.3e4
+ capmod=2 elm=1.87E6 xpart=0 wl=0 wln=1 ww=-4.24558e-15 wwn=1.1141601
wwl=0 wmin=6.5e-7 wmax=4e-3
+ ll=1.8e-15 lln=1.12 lw=0 lwn=1 lwl=0 lmin=5e-7 lmax=1 cgd1=359.114E-12
cgsl=359.114E-12 ckappa=3.5
+ clc=1E-7 cle=0.6 cf=0 cgdo=8.8566E-13 cgso=8.8566E-13 cgbo=1.1E-10
cj=0.97E-3 mj=0.34 pb=0.66
+ cjsw=0.02E-9 mjsw=0.34 pbsw=0.66 cjswg=0.33E-9 rsh=5 mobmod=1 prt=0
noimod=2 ef=1.0 em=4.1e7 noia=1.0E21
```

```

+ noib=4E5 noic=-5E-12)
.model1 pmos1 pmos (tnom=25 tox=0.0086E-6 xj=2.2E-7 nch=1E17 vth0=-0.55
k1=1.1673 k2=-0.2096066 k3=1e-3
+ k3b=11 w0=1e-6 nlx=1e-10 dvt0w=0 dvt1w=5.3e6 dvt2w=-0.032
dvt0=2.6352757 dvt1=0.6450219 dvt2=-0.3717986
+ u0=110.35 ua=9.459179e-10 ub=1.255121e-18 uc=-2.92643e-11
vsat=4.309786e5 a0=0.5509892 ags=0.2412063
+ b0=1.250589e-6 b1=1e-5 keta=-0.0636998 a1=0 a2=1 rdsw=1500
prwg=0.1061034 prwb=0.0470763 wr=1 wint=0.07E-6
+ lint=0.07E-6 dwg=9.619014e-9 dwb=5.19552e-9 voff=-0.1221676
nfactor=0.663588 cit=0 cdsc=-1e-3 cdsd=0
+ cdsdb=2e-3 eta0=0.049832 etab=-0.05 dsub=0.4465817 pclm=2.7300973
pdiblc1 =2.733845e-3 pdiblc2=1e-10
+ pdiblc3=-5 drout=0.070463 pscbe1=1.633765e9 pscbe2=5.018858e-10
pvag=7.8861604 delta=0.01 alpha0=0
+ beta0=30 js=1e-4 jsw=140e-12 ute=-1.4657254 kt1=-0.3121294
kt1l=2.044296e-8 kt2=-0.0581923 ual=1.016123e-10
+ ubl=-4.73524e-18 ucl=-5.6e-11 at=3.3e4 capmod=2 elm=8E6 xpart=0 wl=0
wln=1 ww=-8.26031e-15
+ wwn=1.0903177 wwl=0 wmin=6.5e-7 wmax=4e-3 ll=-5.75866e-17 llm=1.1596373
lw=0 lwn=1 lwl=0 lmin=5e-7
+ lmax=1 cgd1=369.114E-12 cgs1=369.114E-12 ckappa=3 clc=1E-7 cle=0.6 cf=0
cgdo=8.86357e-13 cgso=8.86357e-13
+ cgbo=1.1e-10 cj=0.83E-3 mj=0.18 pb=0.49 cjsw=0.04E-9 mjsw=0.18
pbsw=0.49 cjswg=0.27E-9 rsh=2.22 mobmod=1
+ prt=0 noimod=2 ef=1.0 em=4.1e7 noia=1.0E19 noib=1.3E5 noic=4.4E-11)

* MOSFET SRAM circuit
* 3D MOS: D G S B - NanoTCAD model
Anmos1 2 1 0 0 nmos3D minTimeStep=1e-15
+ deriv3 = [0 0 0]

* MOSFET: D G S B - SPICE models
Mpmos1 2 1 3 3 pmos1 L=0.5u W=4u
Mnmos2 1 2 0 0 nmos1 L=1u W=1u
Mpmos2 1 2 3 3 pmos1 L=0.5u W=4u

*DC voltage supply
Vdd 3 0 DC +3.3V

*Input bias resistance (logical "0")
*Rin 5 0 1e6

*Feedback resistances
*Rfb1 2 4 100k
*Rfb2 1 5 100k

* Init con
.IC V(2)=3.3 V(1)=0
Transient tran stop=1e-7 step=0.1ps errpreset=liberal lteratio=100
+ relref=sigglobal method=traponly maxstep=1e-8

.END

```

Circuit file of 3D TCAD nFET with the spice devices making up the SRAM cell

CFDRC Mixed-mode NanoTCAD simulation with ion strike

```
* 3D NanoTCAD simulation for struck 1-um PMOS device and
* SPICE models for the other 3 transistors in SRAM circuit.

* ACE PMOS 3D model for Spectre
.model pmos3D ACE model="PMOS.DTF"
+ pin1="electric:Sub_epi_DrainContact"
+ pin2="electric:Poly_GateContact"
+ pin3="electric:Sub_epi_SourceContact"
+ pin4="electric:Sub_epi_SubstrateContact"
+ pin5="electric:Sub_epi_WellContact"
+ trace=3 pert=0.1V jacTolV=0.5V jacToli=1e-10 zero=1e-9 tol=2e-2
+ maxTimeStep=[0.3ps 3ps 0.5ps 5ps 1ps 10ps
+ 50ps 250ps 1e-10 1ns 1ns 1e-8 1e-6]
+ maxiter=20 skipFirst=1 maxvoltchg=0.125 currentMult=1

.options VABSTOL=10mV IABSTOL=10nA RELTOL=0.001

* SPICE NMOS and PMOS transistor models, with JUNCTION CAPACITANCES
.model nmos1 nmos (tnom=25 tox=0.0088E-6 xj=2.2E-7 nch=1.7E17 vth0=0.6
k1=0.76016 k2=-5.822152e-4
+ k3=5.0548281 k3b=5.0619266 w0=2.54204e-6 nlx=1.223643e-7 dvt0w=0
dvt1w=5.3e6 dvt2w=-0.032 dvt0=1.8396882
+ dvt1=0.6378645 dvt2=-0.44537 u0=435.0 ua=2e-13 ub=1.755743e-18
uc=9.12133e-11 vsat=1.006979e5
+ a0=1.0566486 ags=0.21 b0=1e-8 b1=9.89043e-8 keta=-4.239715e-3
a1=9.99316e-5 a2=1 rdsw=500
+ prwg=-4.096156e-4 prwb=0.0603814 wr=1 wint=0.12e-6 lint=0.055E-6
dwg=1.205029e-8 dwb=1.599025e-8
+ voff=-0.15 nfactor=1.3428907 cit=0 cdsc=-1e-3 cdsd=0 cdsb=-1e-4
eta0=0.2515419 etab=-0.02 dsub=1
+ pclm=0.5717291 pdiblc1=5.7744e-3 pdiblc2=3.422444e-3 pdiblc3=-0.1625042
drout=0.0851327 pscbe1=4.678648e8
+ pscbe2=5.097051e-4 pvag=0.025509 delta=0.01 alpha0=6.4E-6 beta0=24.5
js=1e-4 jsw=140E-12
+ ute=-1.35868 kt1=-0.3136 kt11=7.3301e-9 kt2=-0.052227 ual=3.01729e-9
ub1=-4.46905e-18 uc1=-5.6e-11 at=3.3e4
+ capmod=2 elm=1.87E6 xpart=0 wl=0 wln=1 ww=-4.24558e-15 wwn=1.1141601
wwl=0 wmin=6.5e-7 wmax=4e-3
+ ll=1.8e-15 llm=1.12 lw=0 lwn=1 lw1=0 lmin=5e-7 lmax=1 cgdl=359.114E-12
cgsl=359.114E-12 ckappa=3.5
+ clc=1E-7 cle=0.6 cf=0 cgdo=8.8566E-13 cgso=8.8566E-13 cgbo=1.1E-10
cj=0.97E-3 mj=0.34 pb=0.66
+ cjsw=0.02E-9 mjsw=0.34 pbsw=0.66 cjswg=0.33E-9 rsh=5 mobmod=1 prt=0
noimod=2 ef=1.0 em=4.1e7 noia=1.0E21
+ noib=4E5 noic=-5E-12)
.model pmos1 pmos (tnom=25 tox=0.0086E-6 xj=2.2E-7 nch=1E17 vth0=-0.55
k1=1.1673 k2=-0.2096066 k3=1e-3
+ k3b=11 w0=1e-6 nlx=1e-10 dvt0w=0 dvt1w=5.3e6 dvt2w=-0.032
dvt0=2.6352757 dvt1=0.6450219 dvt2=-0.3717986
+ u0=110.35 ua=9.459179e-10 ub=1.255121e-18 uc=-2.92643e-11
vsat=4.309786e5 a0=0.5509892 ags=0.2412063
+ b0=1.250589e-6 b1=1e-5 keta=-0.0636998 a1=0 a2=1 rdsw=1500
prwg=0.1061034 prwb=0.0470763 wr=1 wint=0.07E-6
+ lint=0.07E-6 dwg=9.619014e-9 dwb=5.19552e-9 voff=-0.1221676
nfactor=0.663588 cit=0 cdsc=-1e-3 cdsd=0
```

```

+ cdsb=2e-3 eta0=0.049832 etab=-0.05 dsub=0.4465817 pclm=2.7300973
pdiblc1 =2.733845e-3 pdiblc2=1e-10
+ pdiblc3=-5 drout=0.070463 pscbel=1.633765e9 pscbe2=5.018858e-10
pvag=7.8861604 delta=0.01 alpha0=0
+ beta0=30 js=1e-4 jsw=140e-12 ute=-1.4657254 kt1=-0.3121294
kt1l=2.044296e-8 kt2=-0.0581923 ual=1.016123e-10
+ ubl=-4.73524e-18 uc1=-5.6e-11 at=3.3e4 capmod=2 elm=8E6 xpart=0 wl=0
wln=1 ww=-8.26031e-15
+ wwn=1.0903177 wwl=0 wmin=6.5e-7 wmax=4e-3 ll=-5.75866e-17 llm=1.1596373
lw=0 lwn=1 lwl=0 lmin=5e-7
+ lmax=1 cgdl=369.114E-12 cgsl=369.114E-12 ckappa=3 clc=1E-7 cle=0.6 cf=0
cgdo=8.86357e-13 cgso=8.86357e-13
+ cgbo=1.1e-10 cj=0.83E-3 mj=0.18 pb=0.49 cjsw=0.04E-9 mjsw=0.18
pbsw=0.49 cjswg=0.27E-9 rsh=2.22 mobmod=1
+ prt=0 noimod=2 ef=1.0 em=4.1e7 noia=1.0E19 noib=1.3E5 noic=4.4E-11)

* MOSFET SRAM circuit
* 3D MOS: D G S B W - NanoTCAD model
Apmos2 1 2 3 0 3 pmos3D minTimeStep=1e-15
+ deriv3 = [0 0 0]

* MOSFET: D G S B - SPICE models
Mpmos1 2 1 3 3 pmos1 L=0.5u W=4u
Mnmos2 1 2 0 0 nmos1 L=1u W=1u
Mnmos1 2 1 0 0 nmos1 L=1u W=1u

*DC voltage supply
Vdd 3 0 DC +3.3V

*Input bias resistance (logical "0")
*Rin 5 0 1e6

*Feedback resistances
*Rfb1 2 4 100k
*Rfb2 1 5 100k

* Init con
.IC V(2)=3.3 V(1)=0
Transient tran stop=1e-7 step=0.1ps errpreset=liberal lteratio=100
+ relref=sigglobal method=traponly maxstep=1e-8

.END

```

IBM SiGe 5AM Spice Parameters

Spice parameters for nFET with temperatures ranging from 300K to 225K

```

PSET NMOS5AM
DEVICE BSIM3
PARAMETERS

```

```

pmos=0
nmos=1
tnom=25

```

```

tox=0.0088E-6
xj=2.2E-7
nch=1.7E17
line 464
vth0=0.6
k1=0.76016
k2=-5.822152e-4
k3=5.0548281
k3b=5.0619266
w0=2.54204e-6
nlx=1.223643e-7
dvt0w=0
dvt1w=5.3e6
dvt2w=-0.032
dvt0=1.8396882
dvt1=0.6378645
dvt2=-0.44537
u0=435.0
ua=2e-13
ub=1.755743e-18
uc=9.12133e-11
vsat=1.006979e5
a0=1.0566486
ags=0.21
b0=1e-8
b1=9.89043e-8
keta=-4.239715e-3
a1=9.99316e-5
a2=1
rdsw=500
prwg=-4.096156e-4
prwb=0.0603814
wr=1
wint=0.12e-6
lint=0.055E-6
dwg=1.205029e-8
dwb=1.599025e-8
voff=-0.15
nfactor=1.3428907
cit=0
cdsc=-1e-3
cdscd=0
cdscb=-1e-4
eta0=0.2515419
etab=-0.02
dsub=1
pclm=0.5717291
pdiblc1=5.7744e-3
pdiblc2=3.422444e-3
pdiblc3=-0.1625042
drout=0.0851327
pscbe1=4.678648e8
pscbe2=5.097051e-4
pvag=0.025509
delta=0.01
alpha0=6.4E-6
beta0=24.5
js=1e-4
jsw=140E-12
ute=-1.35868
kt1=-0.3136
kt11=7.3301e-9
kt2=-0.052227

```

```

ua1=3.01729e-9
ub1=-4.46905e-18
uc1=-5.6e-11
at=3.3e4
capmod=2
elm=1.87E6
xpart=0
wl=0
wln=1
ww=-4.24558e-15
wn=1.1141601
wwl=0
wmin=6.5e-7
wmax=4e-3
ll=1.8e-15
lln=1.12
lw=0
lwn=1
lwl=0
lmin=5e-7
lmax=1
cgdl=359.114E-12
cgsl=359.114E-12
ckappa=3.5
clc=1E-7
cle=0.6
cf=0
cgdo=8.8566E-13
cgso=8.8566E-13
cgbo=1.1E-10
cj=0.97E-3
mj=0.34
pb=0.66
cjsw=0.02E-9
mjsw=0.34
pbsw=0.66
cjswg=0.33E-9
rsh=5
dsubu diode; Dessis doesn't like this.
nfetest.scs; Dessis doesn't like this
mobmod=1
prt=0
noimod=2
ef=1.0
em=4.1e7
noia=1.0E21
noib=4E5
noic=-5E-12

END PSET

```

Spice parameters for pFET with temperatures ranging from 300K to 225K

```
PSET PMOS5AM
  DEVICE BSIM3
  PARAMETERS

pmos=1
nmos=0
tnom=25
481
tox=0.0086E-6 //sige5am.design_manual.pdf, page 175 says physical tox =
7.8n and this is used in the TCAD simulations.
xj=2.2E-7
nch=1E17
process.scs, line 484
vth0=-0.55
k1=1.1673
k2=-0.2096066
k3=1e-3
k3b=11
w0=1e-6
nlx=1e-10
dvt0w=0
dvt1w=5.3e6
dvt2w=-0.032
dvt0=2.6352757
dvt1=0.6450219
dvt2=-0.3717986
u0=110.35
ua=9.459179e-10
ub=1.255121e-18
uc=-2.92643e-11
vsat=4.309786e5
a0=0.5509892
ags=0.2412063
b0=1.250589e-6
b1=1e-5
keta=-0.0636998
a1=0
a2=1
rds=1500
prwg=0.1061034
prwb=0.0470763
wr=1
wint=0.07E-6
lint=0.07E-6
dwg=9.619014e-9
dwb=5.19552e-9
voff=-0.1221676
nfactor=0.663588
cit=0
cdsc=-1e-3
cdscd=0
cdsch=2e-3
eta0=0.049832
etab=-0.05
dsub=0.4465817
pclm=2.7300973
pdiblc1 =2.733845e-3
pdiblc2=1e-10
```

```

pdiblcb=-5
drout=0.070463
pscbe1=1.633765e9
pscbe2=5.018858e-10
pvag=7.8861604
delta=0.01
alpha0=0
beta0=30
js=1e-4
jsw=140e-12
proces.scs
ute=-1.4657254
kt1=-0.3121294
kt1l=2.044296e-8
kt2=-0.0581923
ual=1.016123e-10
ubl=-4.73524e-18
ucl=-5.6e-11
at=3.3e4
capmod=2
elm=8E6
xpart=0
wl=0
wln=1
ww=-8.26031e-15
wn=1.0903177
wwl=0
wmin=6.5e-7
wmax=4e-3
ll=-5.75866e-17
lln=1.1596373
lw=0
lwn=1
lwl=0
lmin=5e-7
lmax=1
cgdl=369.114E-12
cgsl=369.114E-12
ckappa=3
clc=1E-7
cle=0.6
cf=0
cgdo=8.86357e-13
cgso=8.86357e-13
cgbo=1.1e-10
cj=0.83E-3
mj=0.18
pb=0.49
cjsw=0.04E-9
mjsw=0.18
pbsw=0.49
cjswg=0.27E-9
rsh=2.22
dsubu diode; Dessis doesn't like this.
nfetest.scs; Dessis doesn't like this
mobmod=1
prt=0
noimod=2
ef=1.0
em=4.1e7
noia=1.0E19
noib=1.3E5
noic=4.4E-11

```

END PSET

Spice parameters for nFET with temperatures ranging from 212K to 175K

```
*
*
simulator lang=spectre
inline subckt nfet (d g s b)
  parameters w=0 l=0 as=0 ad=0 ps=0 pd=0 nrd=0 nrs=0 region=2
  dtemp=0 nf=1
    + gcon=1 nqsmod=0
    + mnvthol = (mnvtho*22e-9/((nf*w*l)**0.5))      // mismatch in
NFET vtho
    + nelm = 2.5e6*(1-(2*nlint))
* gcon = gate connection switch (1 for single-ended, and 2 for
double-ended)
* nqsmod = non-quasi-static model switch (0 for off, and 1 for
on)

* Uses skew parameters nlint, nwint, nvtho, ntoxb3, nuob3, nrds,
nk1b3,
*   ncgdl,  ncaje, nmje, nvje,  ncpjc,  ncpje

m0 (d g1 s b) nfetmod w=w l=l as=as ad=ad ps=ps pd=pd \
      nrd=nrd nrs=nrs region=region trise=dtemp
m=nf
r1  g g1  resistor
  + r=1.5*(w-(2-gcon)*(nwint+mnwint))/((nf*gcon*gcon)*(1-
2*(nlint+mnlint)+0.07u))

* -----
* -----
* -----
* -----
* Model NMOS 162K model for L=1um and L=5um, W=10um
* Model fitted to 162K NMOS data 6/29/05
* Model fitted to IBM model simulated results at -55C(218K)
* Model:      BSIM3v3 Modeling Package
* Date:      May 20, 2007
* -----
* -----
* + LEVEL = 8
*
model nfetmod bsim3v3 type=n
+   a0   =   1.266
+   a1   =   0.073
+   a2   =   0.5389
+   acde =   1
+   af   =   1
+   ags  =   0.204
+   alpha0 =   9.02E-06
+   alpha1 =   0
+   at   =   1.65E+04
```

```

+      b0      =      1.00E-08
+      b1      =      9.89E-08
+      beta0   =      26.91
+      binunit =          2
+      capmod  =          3
+      cdsc    =      0.006001
+      cdsclb  =      0.0015
+      cdscl   =      0.0025
+      cf      =      0
+      cgbo    =      1.10E-10
+      cgdl    =      3.59E-10
+      cgdo    =      8.86E-13
+      cgsl    =      3.59E-10
+      cgso    =      8.86E-13
+      cit     =      0
+      cj      =      0.00097
+      cjsw    =      2.00E-11
+      cjswg   =      3.30E-10
+      ckappa  =          3.5
+      clc     =      1.00E-07
+      cle     =      0.6
+      delta   =      0.01
+      dlc     =      5.50E-08
+      drout   =      0.0851
+      dsub    =      0.7012
+      dvt0    =      10
+      dvt0w   =      0
+      dvt1    =      0.423
+      dvt1w   =      5.30E+06
+      dvt2    =      -0.1363
+      dvt2w   =      -0.032
+      dwb     =      1.60E-08
+      dwc     =      1.20E-07
+      dwg     =      1.21E-08
+      ef      =      1
+      elm     =      2.225
+      em      =      4.10E+07
+      eta0    =      5
+      etab    =      2
+      js      =      0.0001
+      jsw     =      1.40E-10
+      k1      =      0.796
+      k2      =      -0.012
+      k3      =      5.055
+      k3b     =      5.062
+      keta    =      -0.0088
+      kf      =      0
+      kt1     =      -0.162
+      kt1l    =      -2.04E-07
+      kt2     =      -0.1348
+      lint    =      5.50E-08
+      ll      =      1.80E-15
+      llc     =      0
+      lln     =      1.12
+      lw      =      0
+      lwc     =      0
+      lw1     =      0

```

```

+      lwlc  =      0
+      lwn   =      1
+      mj     =    0.34
+      mjsw  =    0.34
+      mjswg =    0.33
+      mobmod =        1
+      moin  =    15
+      n      =      1
+      nch   =  3.38E+17
+      nfactor =      1.545
+      ngate =      0
+      nlx   =  1.94E-07
+      noff  =      1
+      noia  =  1.10E+21
+      noib  =  4.00E+05
+      noic  = -5.00E-12
+      noimod =        1
+      paramchk =      1
+      pb    =    0.66
+      pbsw  =    0.66
+      pbswg =    0.66
+      pclm  =    2.441
+      pdiblc1 =      0.003668
+      pdiblc2 =      0.003694
+      pdiblc3 =      1.83
+      prt   = -503.1
+      prwb  =    0.2
+      prwg  =    0.092
+      pscbe1 =      6.14E+08
+      pscbe2 =      0.0003074
+      pvag  =    1.34
+      rdsw  =    460
+      rsh   =      0
+      tcj   =      0
+      tcjsw =      0
+      tcjswg =      0
+      tnom  =   -55
+      tox   =  7.50E-09
+      toxm  =  7.50E-09
+      tpb   =      0
+      tpbsw =      0
+      tpbswg =      0
+      u0    =    459
+      ua    = -1.15E-09
+      ua1   =  3.00E-09
+      ub    =  2.26E-18
+      ub1   = -3.03E-18
+      uc    =  7.80E-11
+      uc1   =  1.25E-10
+      ute   = -0.572
+      vbm   =   -3.3
+      version =      3.2
+      voff  = -0.112
+      voffcv =      0
+      vsat  =  1.09E+05
+      vth0  =    0.649
+      w0    =  2.50E-06

```

```

+      wint  =      1.00E-07
+      wl    =      0
+      wlc   =      0
+      wln   =      1
+      wr    =      1
+      ww    =     -4.25E-15
+      wwc   =      0
+      wwl   =      0
+      wwlc  =      0
+      wwn   =      1.114
+      xj    =     1.50E-07
+      xpart =      0
+      xti   =      3

```

```
ends nfet
```

Spice parameters for pFET with temperatures ranging from 212K to 175K

```

*
simulator lang=spectre
inline subckt pfet (d g s b)
  parameters w=0 l=0 as=0 ad=0 ps=0 pd=0 nrd=0 nrs=0 region=2
  dtemp=0 nf=1
    + gcon=1 nqsmode=0
    + mpvthol = (mpvtho*16e-9/((nf*w*l)**0.5)) // mismatch in
PFET vtho
    + pelm = 8e6*(1-(2*plint))
* gcon = gate connection switch (1 for single-ended, and 2 for
double-ended)
* nqsmode = non-quasi-static model switch (0 for off, and 1 for
on)

* Uses skew parameters plint, pwint, pvtho, ntoxb3, puob3, prdsw,
pk1b3,
*      pcgdl, pcaje, pmje, pvje, pcpcj, pcpcje

m0 (d g1 s b) pfetmod w=w l=l as=as ad=ad ps=ps pd=pd \
                                nrd=nrd nrs=nrs region=region trise=dtemp
m=nf
r1 g g1 resistor
  + r=1.5*(w-(2-gcon)*(pwint+mpwint))/((nf*gcon*gcon)*(1-
2*(plint+mplint)+0.10u))

model pfetmod bsim3v3 type=p
+      a0      =      0.732
+      a1      =      0.015
+      a2      =      0.1195
+      acde    =      1
+      af      =      1.5
+      ags     =      0.252
+      alpha0   =     5.00E-13
+      alpha1   =      0
+      at      =     5.00E+04
+      b0      =      0

```

```

+      b1      =      0
+      beta0   =     35.4
+      binunit =         2
+      capmod  =         3
+      cdsc    =     1.00E-06
+      cds cb  =     7.59E-06
+      cds cd  =     0.001365
+      cf      =      0
+      cgbo    =      0
+      cgdl    =      0
+      cgdo    =      0
+      cgsl    =      0
+      cgso    =      0
+      cit     =      0
+      cj      =     0.0005
+      cjsw    =     5.00E-10
+      cjswg   =     5.00E-10
+      ckappa  =         0.6
+      clc     =     1.00E-07
+      cle     =     0.6
+      delta   =     0.01
+      dlc     =      0
+      drout   =     0.56
+      dsub    =     0.56
+      dvt0    =     7.896
+      dvt0w   =      0
+      dvt1    =     0.3672
+      dvt1w   =     5.30E+06
+      dvt2    =    -0.09073
+      dvt2w   =    -0.032
+      dwb     =      0
+      dwc     =      0
+      dwg     =      0
+      ef      =     1.5
+      elm     =      2
+      em      =     4.10E+07
+      eta0    =      0
+      etab    =     -2
+      js      =     0.0001
+      jsw     =     1.00E-12
+      k1      =     1.174
+      k2      =    -0.223
+      k3      =      0
+      k3b     =      0
+      keta    =    -0.0692
+      kf      =     1.00E-17
+      kt1     =    -0.252
+      kt11    =     2.40E-08
+      kt2     =     0.0244
+      lint    =      0
+      ll      =      0
+      llc     =      0
+      lln     =      1
+      lw      =      0
+      lwc     =      0
+      lw1     =      0
+      lwlc    =      0

```

```

+   lwn   =   1
+   mj    =   0.5
+   mjsw  =   0.33
+   mjswg =   0.33
+   mobmod =      1
+   moin  =   15
+   n     =   1
+   nch   =   1.89E+17
+   nfactor =      1.545
+   ngate =   0
+   nlx   =   4.44E-22
+   noff  =   1
+   noia  =   2.00E+29
+   noib  =   5.00E+04
+   noic  =  -1.40E-12
+   noimod =      1
+   paramchk =      1
+   pb    =   1
+   pbsw  =   1
+   pbswg =   1
+   pclm  =   9.92
+   pdiblc1 =      0.01336
+   pdiblc2 =      2.18E-09
+   pdiblc3 =      5
+   prt   =  -400
+   prwb  =  -1
+   prwg  =   0.2147
+   pscbe1 =      2.11E+08
+   pscbe2 =      1.00E-07
+   pvag  =   0
+   rdsw  =  110.3
+   rsh   =   0
+   tcj   =   0
+   tcjsw =   0
+   tcjswg =      0
+   tnom  =  -55
+   tox   =   7.50E-09
+   toxm  =   7.50E-09
+   tpb   =   0
+   tpbsw =   0
+   tpbswg =      0
+   u0    =  128
+   ua    =  -2.18E-10
+   ua1   =   4.57E-10
+   ub    =   2.92E-18
+   ub1   =  -2.40E-18
+   uc    =   7.99E-12
+   uc1   =   2.30E-12
+   ute   =  -1.088
+   vbm   =  -3.3
+   version =      3.2
+   voff  =  -0.08
+   voffcv =      0
+   vsat  =   7.51E+05
+   vth0  =  -0.636
+   w0    =   2.50E-06
+   wint  =   0

```

```

+      wl      =      0
+      wlc     =      0
+      wln     =      1
+      wr      =      1
+      ww      =      0
+      wwc     =      0
+      wwl     =      0
+      wwlc    =      0
+      wwn     =      1
+      xj      =      1.50E-07
+      xpart   =      0.5
+      xti     =      3

```

```
ends pfet
```

Spice parameters for nFET with temperatures ranging from 150K to 125K

```

simulator lang=spectre
inline subckt nfet (d g s b)
  parameters
    + w      = 0
    + l      = 0
    + as     = 0
    + ad     = 0
    + ps     = 0
    + pd     = 0
    + nrd    = 0
    + nrs    = 0
    + region = 2
    + dtemp  = 0
    + nf     = 1
    + nqsmod = 0
    + gcon   = 1
    + mnvtho1 = (mnvtho*22e-9/((nf*w*l)**0.5)) // mismatch in
NFET vtho
    + nelm = 2.5e6*(1-(2*nlint))

  m0 (d g1 s b) nfetmod
    + w      = w
    + l      = l
    + as     = as
    + ad     = ad
    + ps     = ps
    + pd     = pd
    + nrd    = nrd
    + nrs    = nrs
    + region = region
    + trise  = dtemp
    + m      = nf

  r1 g g1 resistor
    + r=1.5*(w-(2-gcon)*(nwint+mnwint))/((nf*gcon*gcon)*(1-
2*(nlint+mnlint)+0.07u))

```

```

model nfetmod bsim3v3
+ type      = n
+ version   = 3.2
+ a0        = 876.0E-3
+ a1        = 1.000E-12
+ a2        = 1.000
+ acde      = 1.000
+ af        = 1.000
+ ags       = 252.0E-3
+ alpha0    = 6.400E-6
+ alpha1    = 0.000
+ at        = 43.00E3
+ b0        = 10.00E-9
+ b1        = 98.90E-9
+ beta0     = 24.50
+ binunit   = 1.000
+ capmod    = 2.000
+ cdsc      = 146.0E-3
+ cdsch     = 38.00E-3
+ cdschd    = -7.000E-3
+ cf        = 0.000
+ cgbo      = 110.0E-12
+ cgd1      = 359.0E-12
+ cgdo      = 886.0E-15
+ cgsl      = 359.0E-12
+ cgso      = 886.0E-15
+ cit       = 0.000
+ cj        = 970.0E-6
+ cjsw      = 20.00E-12
+ cjswg     = 330.0E-12
+ ckappa    = 3.500
+ clc       = 100.0E-9
+ cle       = 600.0E-3
+ delta     = 10.00E-3
+ dlc       = 55.00E-9
+ drout     = 85.10E-3
+ dsub      = 1.000
+ dvt0      = 821.3E-3
+ dvt0w     = 0.000
+ dvt1      = 1.000
+ dvt1w     = 5.300E6
+ dvt2      = -935.9E-3
+ dvt2w     = -32.00E-3
+ dwb       = 16.00E-9
+ dwc       = 120.0E-9
+ dwg       = 12.10E-9
+ ef        = 1.000
+ elm       = 2.225
+ em        = 41.00E6
+ eta0      = 252.0E-3
+ etab      = -20.00E-3
+ js        = 100.0E-6
+ jsw       = 140.0E-12
+ k1        = 857.4E-3
+ k2        = -61.48E-3
+ k3        = 5.055
+ k3b       = 5.062

```

```

+ keta      = -24.40E-3
+ kf        = 0.000
+ kt1       = -284.0E-3
+ kt11      = -138.0E-9
+ kt2       = -14.80E-3
+ lint      = 55.00E-9
+ ll        = 1.800E-15
+ llc       = 0.000
+ lln       = 1.120
+ lw        = 0.000
+ lwc       = 0.000
+ lwl       = 0.000
+ lwlc      = 0.000
+ lwn       = 1.000
+ mj        = 340.0E-3
+ mjsw      = 340.0E-3
+ mjswg     = 330.0E-3
+ mobmod    = 1.000
+ moin      = 15.00
+ n         = 1.000
+ nch       = 1.93818E+017
+ nfactor   = 1.714
+ ngate     = 0.000
+ nlx       = 102.0E-9
+ noff      = 1.000
+ noia      = 1.10000E+021
+ noib      = 400.0E3
+ noic      = -5.000E-12
+ noimod    = 2.000
+ paramchk  = 1.000
+ pb        = 660.0E-3
+ pbsw      = 660.0E-3
+ pbswg     = 660.0E-3
+ pclm      = 1.381
+ pdiblc1   = 1.000E-3
+ pdiblc2   = 3.420E-3
+ pdiblc3   = -930.0E-3
+ prt       = -430.0
+ prwb      = -107.0E-3
+ prwg      = -117.0E-3
+ pscbe1    = 481.8E6
+ pscbe2    = 510.0E-6
+ pvag      = 0.000
+ rdsw      = 911.9
+ rsh       = 5.000
+ tcj       = 0.000
+ tcjsw     = 0.000
+ tcjswg    = 0.000
+ tnom      = -111.0
+ tox       = 8.800E-9
+ toxm      = 8.800E-9
+ tpb       = 0.000
+ tpbsw     = 0.000
+ tpbswg    = 0.000
+ u0        = 593.0
+ ua1       = 2.205E-9
+ ua        = -2.250E-9

```

```

+ ub1      = -4.924E-18
+ ub       = 3.800E-18
+ uc1      = 500.0E-15
+ uc       = 15.85E-12
+ ute      = -1.050
+ vbm      = -3.300
+ voff     = -112.0E-3
+ voffcv   = 0.000
+ vsat     = 85.33E3
+ vth0     = 694.9E-3
+ w0       = 2.500E-6
+ wint     = 100.0E-9
+ wl       = 0.000
+ wlc      = 0.000
+ wln      = 1.000
+ wr       = 1.000
+ ww       = -4.250E-15
+ wwc      = 0.000
+ wwl      = 0.000
+ wwlc     = 0.000
+ wwn      = 1.114
+ xj       = 230.0E-9
+ xpart    = 0.000
+ xti      = 3.000
// ijth    = 100.0E-3      unused
// level   = 8.000        unused
ends nfet

```

Spice parameters for pFET with temperatures ranging from 150K to 125K

```

simulator lang=spectre
inline subckt pfet (d g s b)
parameters
+ w      = 0
+ l      = 0
+ as     = 0
+ ad     = 0
+ ps     = 0
+ pd     = 0
+ nrd    = 0
+ nrs    = 0
+ region = 2
+ dtemp  = 0
+ nf     = 1
+ gcon   = 1
+ nqsmod = 0
+ mpvtho1 = (mpvtho*16e-9/((nf*w*l)**0.5)) // mismatch in
PFET vtho
+ pelm   = 8e6*(1-(2*plint))

m0 (d g1 s b) pfetmod
+ w      = w
+ l      = l
+ as     = as
+ ad     = ad

```

```

+ ps      = ps
+ pd      = pd
+ nrd     = nrd
+ nrs     = nrs
+ region  = region
+ trise   = dtemp
+ m       = nf

r1 g g1 resistor
+ r=1.5*(w-(2-gcon)*(pwint+mpwint))/((nf*gcon*gcon)*(1-
2*(plint+mplint)+0.10u))

model pfetmod bsim3v3
+ type      = p
+ version   = 3.2
+ a0        = 636.0E-3
+ a1        = 49.00E-3
+ a2        = 995.0E-3
+ acde      = 1.000
+ af        = 1.000
+ ags       = 362.8E-3
+ alpha0    = -10.00E-6
+ alpha1    = 100.0
+ at        = 500.0
+ b0        = 1.251E-6
+ b1        = 10.00E-6
+ beta0     = 43.60
+ binunit   = 2.000
+ capmod    = 3.000
+ cdsc      = 1.000E-6
+ cdschb    = -999.4E-3
+ cdschd    = 0.000
+ cf        = 0.000
+ cgbo      = 110.0E-12
+ cgdl      = 3.691E-12
+ cgdo      = 8.864E-15
+ cgsl      = 3.690E-12
+ cgso      = 8.864E-15
+ cit       = 0.000
+ cj        = 830.0E-6
+ cjsw      = 40.00E-12
+ cjswg     = 270.0E-12
+ ckappa    = 3.000
+ clc       = 100.0E-9
+ cle       = 600.0E-3
+ delta     = 10.00E-3
+ dlc       = 70.00E-9
+ drout     = 7.050E-3
+ dsub      = 361.9E-3
+ dvt0      = 9.418
+ dvt0w     = 0.000
+ dvt1      = 1.288
+ dvt1w     = 5.300E6
+ dvt2      = 296.3E-3
+ dvt2w     = -32.00E-3
+ dwb       = 5.200E-9
+ dwc       = 70.00E-9

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+ dwg      = 9.620E-9
+ ef       = 1.000
+ elm      = 6.880
+ em       = 41.00E6
+ eta0     = 2.220E-15
+ etab     = -142.7E-3
+ js       = 100.0E-6
+ jsw      = 140.0E-12
+ k1       = 1.220
+ k2       = -220.0E-3
+ k3       = 1.000E-3
+ k3b      = 11.00
+ keta     = -45.18E-3
+ kf       = 0.000
+ kt1      = -90.00E-3
+ kt11     = 20.40E-9
+ kt2      = 14.40E-3
+ lint     = 70.00E-9
+ ll       = -57.59E-18
+ llc      = 0.000
+ lln      = 1.160
+ lw       = 0.000
+ lwc      = 0.000
+ lwl      = 0.000
+ lwlc     = 0.000
+ lwn      = 1.000
+ mj       = 180.0E-3
+ mjsw     = 180.0E-3
+ mjswg    = 330.0E-3
+ mobmod   = 1.000
+ moin     = 15.00
+ n        = 1.700
+ nch      = 1.93460E+017
+ nfactor  = 901.9E-3
+ ngate    = 0.000
+ nlx      = 4.44100E-022
+ noff     = 1.000
+ noia     = 1.000000E+019
+ noib     = 130.0E3
+ noic     = 44.00E-12
+ noimod   = 1.000
+ paramchk = 1.000
+ pb       = 490.0E-3
+ pbsw     = 490.0E-3
+ pbswg    = 490.0E-3
+ pclm     = 4.311
+ pdiblc1  = 1.000E-3
+ pdiblc2  = 1.444E-15
+ pdiblcb  = -690.0E-3
+ prt      = 0.000
+ prwb     = -838.0E-3
+ prwg     = 269.0E-3
+ pscbe1   = 331.8E6
+ pscbe2   = 13.27E-6
+ pvag     = 2.560
+ rdsw     = 950.0
+ rsh      = 0.000

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+ tcj      = 0.000
+ tcjsw    = 0.000
+ tcjswg   = 0.000
+ tnom     = -111.0
+ tox      = 7.500E-9
+ toxm     = 7.500E-9
+ tpb      = 0.000
+ tpbsw    = 0.000
+ tpbswg   = 0.000
+ u0       = 162.0
+ ual      = 680.1E-12
+ ua       = -430.0E-12
+ ub1      = -2.590E-18
+ ub       = 3.060E-18
+ ucl      = 800.0E-15
+ uc       = -35.00E-12
+ ute      = -465.0E-3
+ vbm      = -3.300
+ voff     = -112.0E-3
+ voffcv   = 0.000
+ vsat     = 86.97E3
+ vth0     = -687.8E-3
+ w0       = 1.000E-6
+ wint     = 70.00E-9
+ wl       = 0.000
+ wlc      = 0.000
+ wln      = 1.000
+ wr       = 1.000
+ ww       = -8.260E-15
+ wwc      = 0.000
+ wwl      = 0.000
+ wwlc     = 0.000
+ wwn      = 1.090
+ xj       = 150.0E-9
+ xpart    = 0.000
+ xti      = 3.000
// ijth    = 100.0E-3      unused
// level   = 8.000        unused
ends pfet

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